Study Of Cu Free Back Contacts To Thin Film CdTe Solar Cells

by

Vijay Viswanathan

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
Department of Electrical Engineering
College of Engineering
University of South Florida

Major Professor: Christos. S. Ferekides, Ph.D
Don Morel, Ph.D
Richard Gilbert, Ph.D
Y.L. Chiou, Ph.D
Sarath Witanachchi, Ph.D

Date of Approval:
February 2, 2004

Keywords: CdTe, Contacts, Ni-P, ZnTe, Dry Etching, Stability.

DEDICATION

This dissertation is dedicated to my parents and sisters for their love and encouragement throughout this dissertation, and my loving wife for her support in the final stages of this work.

ACKNOWLEDGMENTS

I would like to express my gratitude to my major professor, Dr. Chris Ferekides, for his invaluable guidance and support during this project. I also thank Dr. Don Morel for all of his help and guidance over the past years. I would like to thank all the other committee members: Dr. Sarath Witanachchi, Dr. Yun-Leei Chiou, and Dr. Richard Gilbert for their help in the course of the fulfillment of my dissertation, and Dr. A.N.V Rao for chairing my dissertation defense.

I also like to thank Sally Asher at NREL for her help with SIMS characterization, Dr Brian McCandless at Georgia State University for his help with GIXRD measurements, and Isaiah Oladeji (University of Central Florida) for SIMS analysis.

I would like to express my special thanks to the fellow research assistants at semiconductor lab: B. Tetali, V. Komin, Zhiyong Zhao, V. Palekis, R. Mamazza, S. Jagannathan, P. Selvaraj and N. Rao.

Finally I would like to thank all my roommates for their moral support and motivation.

This work was supported by National Renewable Energy Laboratory (NREL), US Department of Energy.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

STUDY OF CU FREE BACK CONTACTS TO THIN FILM CDTE SOLAR CELLS

by

Vijay Viswanathan

ABSTRACT

The goals of this project are study Cu free back contact alternatives for CdS/CdTe thin film solar cells, and to research dry etching for CdTe surface preparation before contact application. In addition, an attempt has been made to evaluate the stability of some of the contacts researched. The contacts studied in this work include ZnTe/Cu_2Te, Sb_2Te_3, and Ni-P alloys.

The ZnTe/Cu_2Te contact system is studied as basically an extension of the earlier work done on Cu_2Te at USF. RF sputtering from a compound target of ZnTe and Cu_2Te respectively deposits these layers on etched CdTe surface. The effect of Cu_2Te thickness and deposition temperature on contact and cell performance will be studied with the ZnTe depositions conditions kept constant. C-V measurements to study the effect of contact deposition conditions on CdTe doping will also be performed. These contacts will then be stressed to high temperatures (70-100 ^oC) and their stability with stress time is analyzed.

Sb_2Te_3 will be deposited on glass using RF sputtering, to study film properties with deposition temperature. The Sb_2Te_3 contact performance will also be studied as a function of the Sb_2Te_3 deposition temperature and thickness.

The suitability of Ni-P alloys for back contacts to CdTe solar cells was studied by forming a colloidal mixture of Ni_2P in graphite paste. The Ni-P contacts, painted on Br-methanol etched CdTe surface, will be studied as a function of Ni-P concentration (in the graphite paste), annealing temperature and time. Some of these cells will undergo temperature stress testing to determine contact behavior with time.

Dry etching of CdTe will be studied as an alternative for wet etching processes currently used for CdTe solar cells. The CdTe surface is isotropically etched in a barrel reactor in N_2, Ar or $Ar:O_2$ ambient. The effect of etching ambient, pressure, plasma power and etch time on contact performance will be studied.

CHAPTER 1

INTRODUCTION

The industrial revolution of the nineteenth century spawned a new age of technology that placed increasing emphasis on energy for its growth. Fossils fuels like coal, oil and gas, the conventional sources of energy, fueled the development of this technology. However at the present time these sources are dwindling, and can no longer support the ever-increasing demand. The search for other non-conventional sources of energy has thus gained increased attention. In particular, the use of renewable energy sources that are essentially non-polluting provides an attractive alternative.

1.1 Non-Conventional Energy Sources

These include hydroelectric power, solar energy, nuclear, tidal and geothermal energy. Although nuclear energy is a very attractive alternative, the promise of obtaining large amounts of inexpensive clean energy has not become a reality. This has been primarily due to the risks associated with nuclear reactors, which are centered around the effect of ionizing radiation on the health of people dwelling near the nuclear plant (one is reminded of the Chernobyl disaster). In addition, the cost involved in construction, maintenance, and proper disposal of radioactive wastes have made utilities invest in less expensive substitutes to meet the energy demands of the world. Although hydroelectric

power and wind power have been harnessed, the potential of these forms to satisfy the energy needs is questionable. The Sun has been worshipped as a life-giver to our planet since ancient times. The energy received from the sun on earth's surface is 1.2×10^{17} on an average. This means that in less than one hour enough energy is supplied to the earth to satisfy the entire energy need of the human population for the whole year. The conversion of sunlight directly into electricity using the photovoltaic properties of suitable materials is the most elegant energy conversion process. Table 1 [1] at the end of this chapter provides an overall picture of the various alternative resources available with its advantages and shortcomings.

1.2 Solar Cells – A Historical Background

The photovoltaic effect discovered by Edmund Becquerel in 1839 lies at the heart of the operation of a solar cell. He observed that metal plates immersed into a suitable electrolyte, when exposed to sunlight, produced a small voltage and current. The first solid-state material to exhibit photovoltaic behavior was Selenium in 1876 and later cuprous oxide, indicating that semiconductors would be the material of choice in the future. Major development began with the fabrication of diffused p-n junctions in 1954, while at the same time the initial success was obtained for the Cu_2S/CdS heterojunction.

With the advent of space exploration, the need for a reliable long lasting power source led to one of the major applications of solar cells, namely the space shuttle. The increasing demand for energy, the crisis in the Middle East in the 1970's, and the oil embargo raised interest in solar cells as an alternative source for terrestrial applications.

This led to improvements in device efficiencies, reduction of energy cost, and the research and development of other materials for photovoltaics.

Since the 1980's new solar cell materials, and innovative device concepts, have given a new lease to its future development. However the widespread use of solar cells has not been realized due to the reduced efficiencies obtainable in modules fabricated at the present time.

1.3 Semiconductors For Solar Cells

Silicon, being the most researched semiconductor, was the first to be used commercially for solar cells. However it presented certain limitations for terrestrial applications. Silicon has an indirect bandgap and is thus characterized by a low absorption coefficient. Thus a relatively larger thickness is needed to absorb the incident light completely. This leads to the need of obtaining a high purity material to enable carriers (free electrons and holes) to be collected. These results in the increase in fabrication costs associated with the use of complex equipments for growing pure materials. In addition there is a large discrepancy in the efficiencies of small area laboratory cell (about 23%) and modules (10-13%).

In order to be cost competitive alternate low-cost technologies have been sought at the expense of high efficiency. Polycrystalline materials, which afford easier fabrication procedures, have gained increased importance in the last couple of decades. Another approach to the cost problem is the use of compound semiconductors like Cadmium Telluride(CdTe), Copper Indium Selenide(CIS), Gallium Arsenide(GaAs), Indium Phosphide(InP), Cadmium Selenide(CdSe). All these semiconductors

characterized by a high absorption coefficient due to the direct bandgap. In addition their bandgap closely match the solar spectrum to facilitate efficient utilization. The advantage of possessing a high absorption is the lack of need to grow a thick layer for complete light absorption, as in the case of silicon. Thus the loss of carriers to recombination is reduced and thus places less emphasis on the purity of the material. Another advantage to the use of these materials is the wide range of techniques like MOCVD, MBE, sputtering, evaporation, available for the growth of these films. Also since the films are polycrystalline, low-cost substrates like polymers and glass could be used. Despite the flexibility afforded by these materials, the quality of the films obtained need improvements to facilitate extensive use in terrestrial applications. However novel structures have evolved which provide great promise.

In an effort to further reduce the cost of photovoltaics better utilization of the sunlight has evolved over the years. In the first method, spectrum splitting, the sunlight is directed on the appropriate cell by spectrally sensitive mirrors. In the tandem cell approach, semiconductors of different bandgaps are stacked on one another. For instance, a wider band gap material uses the blue part of the solar spectrum whereas the red part with longer wavelengths passes through and is absorbed by the lower cell with a smaller band gap. Another possible approach to reduce the cost of photovoltaic systems is to concentrate the sunlight on the active area of the solar cell using lenses, mirrors and sun tracking systems.

The research of the last few decades is making the promise of solar energy a reality with a number of companies investing in research, development, and manufacture of devices. The first decade of the new millennium will decide the future of solar power.

1.4 CdTe Solar Cell Technology

Cadmium telluride is one of the leading candidates for low cost thin film photovoltaics. Laboratory efficiencies in excess of 15%[2] and module performance of over 10% making it a very promising candidate for large scale applications. In addition, cells with efficiencies of over 11% have been obtained using a variety of deposition methods. In order to make this potential a reality, however, involves understanding of key issues that limit device performance and reliability. Major focus on further development of these devices revolves around the challenge involving fabrication of a good, stable ohmic contact to CdTe. This is encountered primarily due to its high work function. This is further complicated by the inability to obtain sufficient p-type doping in polycrystalline CdTe.

Copper, the most widely used contact material, suffers from stability issues believed to be caused by its diffusion into the metallurgical junction with time thereby degrading performance and reliability. Although the theory of copper diffusion is quite speculative and needs more systematic studies to understand and quantify its effects, one of the major areas of research is the search for alternative materials for back contacts. Some of the materials researched earlier include ZnTe:Sb, HgTe, PbTe, Li, Ag, and other high workfunction metals like Ni and even Mo, however their reliability and performance are not adequate. A more detailed account of the problem of CdTe contact formation and various contact materials used are presented in chapter 3.

The continued search for alternative materials over the years have provided new materials like Sb_2Te_3 and Ni:P alloys to be promising candidates. To address this pivotal issue, this work studies the feasibility of these new materials for contact fabrication.

Table 1 Table Comparing Various Energy Sources

Present & Future Energy Sources

Energy Source	Types of processes	Advantages	Disadvantages
Petroleum	Drilling, oil shale	Convenient, low pollution	Limited supply, nonrenewable (20 year supply)
Natural Gas	Drilling	Convenient, low pollution	Very limited supply, nonrenewable (5-10 year supply)
Coal	Deep or strip mining, solvent refining, pyrolysis, gasification, magnetohydrodynamic usage	Easy to handle, provides source of hydrocarbons in gaseous or liquid form as well as normal solid form	Atmospheric pollution, nonrenewable, much research needed for production of power by unconventional means (200-300 year supply)
Nuclear Fission	Light-water reactors	Existing technology, compact	Limited fuel supply, thermal pollution, operating and transport hazards, storage of wastes
Breeder Reactors	Liquid-metal-cooled reactors	Reduces limitation of fuel availability	As for nuclear fission, but generally more severe
Nuclear Fusion	Magnetic containment, laser initiated	Unlimited fuel supply	Much materials research needed, radiation leakage problems
Solar Thermal	Direct heating and cooling via absorption of solar radiation	Pollution-free unlimited energy source	Need for extensive architectural changes, storage required
Solar Thermal: electric	Use of solar energy to operate a steam turbine	Pollution-free unlimited energy source	Research needed on collection, focusing and storage
Solar Photovoltaic	Photovoltaic effect in semiconductor junction devices	Pollution-free unlimited energy source	Present high cost of cells, energy storage, and operating lifetime
Hydroelectric	Fall of water under gravity used to generate electricity	Renewable, inexpensive, can be used as storage process, large potential in Third World	Limited to special locations, most of which in U.S. have been developed
Tidal Energy	Motion of water under gravitational pull of moon used to generate electricity	Pollution-free, renewable	Limited number of exploitable sites
Wind	Force of the wind used to generate electricity	Pollution-free, renewable	Limited to special locations, large scale effect on weather unknown, storage required
Ocean Thermal	Uses thermal gradients to drive heat engine and generate electrical energy	Pollution-free, renewable	Special materials problems in resisting corrosion, costly transmission
Geothermal	Decay of radioactive materials within the earth produce heat	Inexpensive	Limited to special locations, corrosion problems, non-renewable
Biomass	Conversion of solid organic matter into synthetic fuel	Ready supply, could utilize wastes	Uses arable land if deliberately planted, cost uncertain, sludge disposal

CHAPTER 2

SEMICONDUCTORS AND SOLAR CELLS

2.1 Semiconductors

A semiconductor is a material whose conductivity lies between the highly conductive metal and the highly resistive insulator. There are a number of ways in which semiconductors can be classified; some of them are listed below.

1) Intrinsic and Extrinsic, based on purity.

2) N-type and P-type, based on whether the majority charge carriers are electrons or holes.

3) Single-crystalline, poly-crystalline and amorphous, based on their structure.

One of the reasons for the extensive use of semiconductors for a wide variety of applications is the ability to change their conductivity by the process of doping. Doping is a process of adding impurities to semiconductors to increase their conductivity by increasing the number of electrons (in the case of N-type) or holes (in the case of P-type). For example, the addition of a group V element to Si provides an additional electron thereby doping it N-type. Similarly a group III element dopes Si P-type by providing an extra hole. The conductivity can also be increased by thermal or optical excitation. Semiconductors are used for the manufacture of a number of devices like p-n junction

diodes, transistors, and MOSFETs, which have revolutionized the technological development over the past half a century.

2.2 Junctions

Junctions are formed when two materials are brought in intimate contact with each other. Homojunctions are formed when the two materials joined together are of the same type whereas two dissimilar materials on contact produce a heterojunction.

There are a number of other ways in which junctions are classified. In this chapter we discuss some of the junctions of interest.

2.3 Metal- Semiconductor Junctions

In most cases it is required to deposit metal over a semiconductor in order to form a contact. The contact thus formed between the two can either be

1) Rectifying (Schottky barriers)

2) Ohmic.

2.3.1 Schottky Barriers

Let us first consider the case of an ideal metal -semiconductor junction. The band diagrams of a metal and N-type semiconductor is shown in figure 1(a). Each metal has a characteristic work function, which is defined as the energy required toremove an electron at the fermi level to the vacuum outside the metal. When a metal with work-function $q\phi_m$

is brought in contact with a n-type semiconductor having a work function $q\phi_s$ charge transfer occurs until the fermi levels align at equilibrium as shown in figure 1(b).

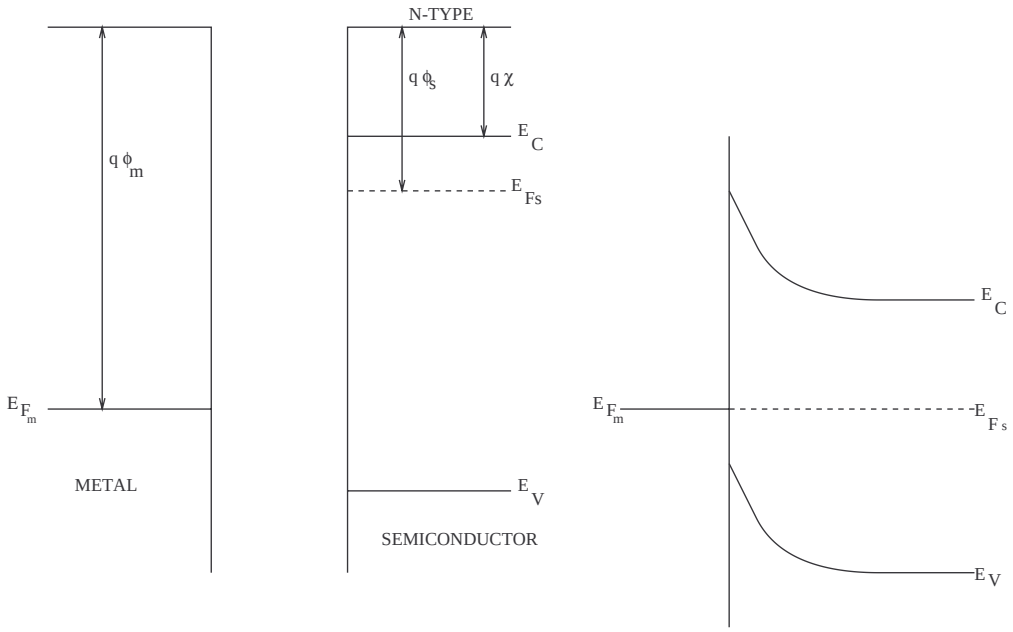


Figure 1 (a) Band Diagrams of Metal and Semiconductor before Junction Formation, (b) After the Junction Formation

In order to align the fermi levels the electrostatic potential of the n-type semiconductor needs to be raised in relation to the metal. Just as in the case of a p-n junction a depletion layer is formed near the junction. The positive charge due to the uncompensated donor ions in the semiconductor is balanced by the excess electrons in the metal. The difference in the work function cause the bands to bend and gives rise to the contact potential V_o. This prevents further net electron diffusion from the semiconductor

into the metal. The potential barrier height ϕ_b for electron injection from the metal to the semiconductor conduction band is $\phi_m - \chi$, where $q\chi$, is the electron affinity (measured from the vacuum level to the semiconductor conduction band).

2.3.1.1 The Current/Voltage Characteristics

The process that determines the current in a metal-semiconductor junction to which a bias is applied is the flow of electrons over the top of the barrier from the semiconductor to the metal and vice-versa. In the absence of bias the current density J_{sm} due to the electrons passing from the semiconductor to the metal must be equal and opposite to that of the electrons passing from the metal to the semiconductor, J_{ms}. When a schottky barrier is forward biased (metal is positive with respect to n-type semiconductor) as shown in figure 2(a) using a voltage V, the bands in the semiconductor are raised in energy relative to the metal and the electric field reduces. Since the conductivity of the metal is many orders of magnitude greater than the semiconductor the reduction of field takes place almost entirely in the semiconductor. As a consequence electrons in the conduction band of the semiconductor can more easily overcome the barrier thereby increasing J_{sm}. However the barrier encountered by the electrons from the metal does not change nad hence J_{ms} is constant. This is the *forward* or *easy* direction of current flow. On application of a reverse bias of the same magnitude, as shown in figure 2(b), the barrier increases by a value V_0 + V. Thus the number of electrons that can surmount the barrier from the semiconductor decreases, that is, ie J_{sm} is greatly reduced while J_{ms} remains constant. However large the applied reverse bias may be, J_{sm} cannot be less than zero, so

the net current saturates at the value J_{ms}, which is independent of the bias voltage. This is the *hard* or *reverse* direction of current flow.

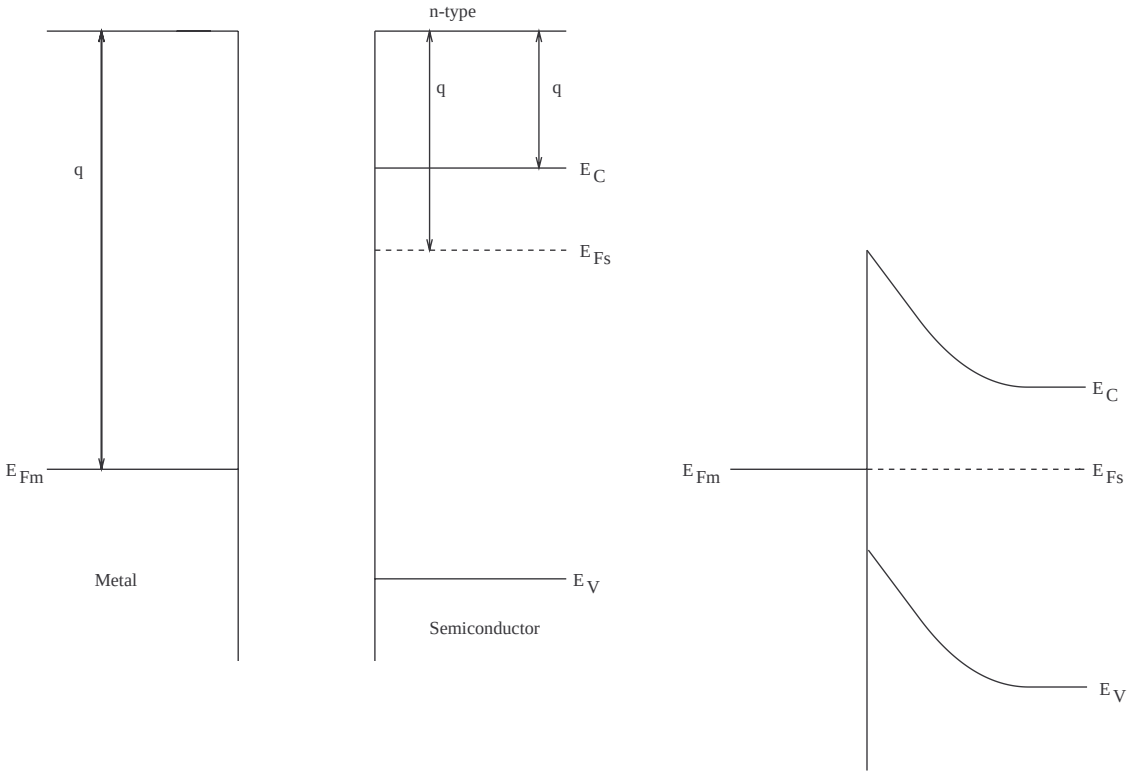


Figure 2 Schottky Barrier (a) Forward Bias, (b) Reverse Bias

2.3.1.2 The Effect of Surface States

In the case of an ideal metal-semiconductor junction the barrier height φ_b depends on the metal work function. However, in practice it is found to be less sensitive to φ_m and under certain conditions φ_b may be almost independent of the choice of the metal.

An explanation of this weak dependence on φm is due to the effect of surface states. Figure 3(a)&(b) show the effect of surface states on the semiconductor surface and the metal -semiconductor barrier respectively.

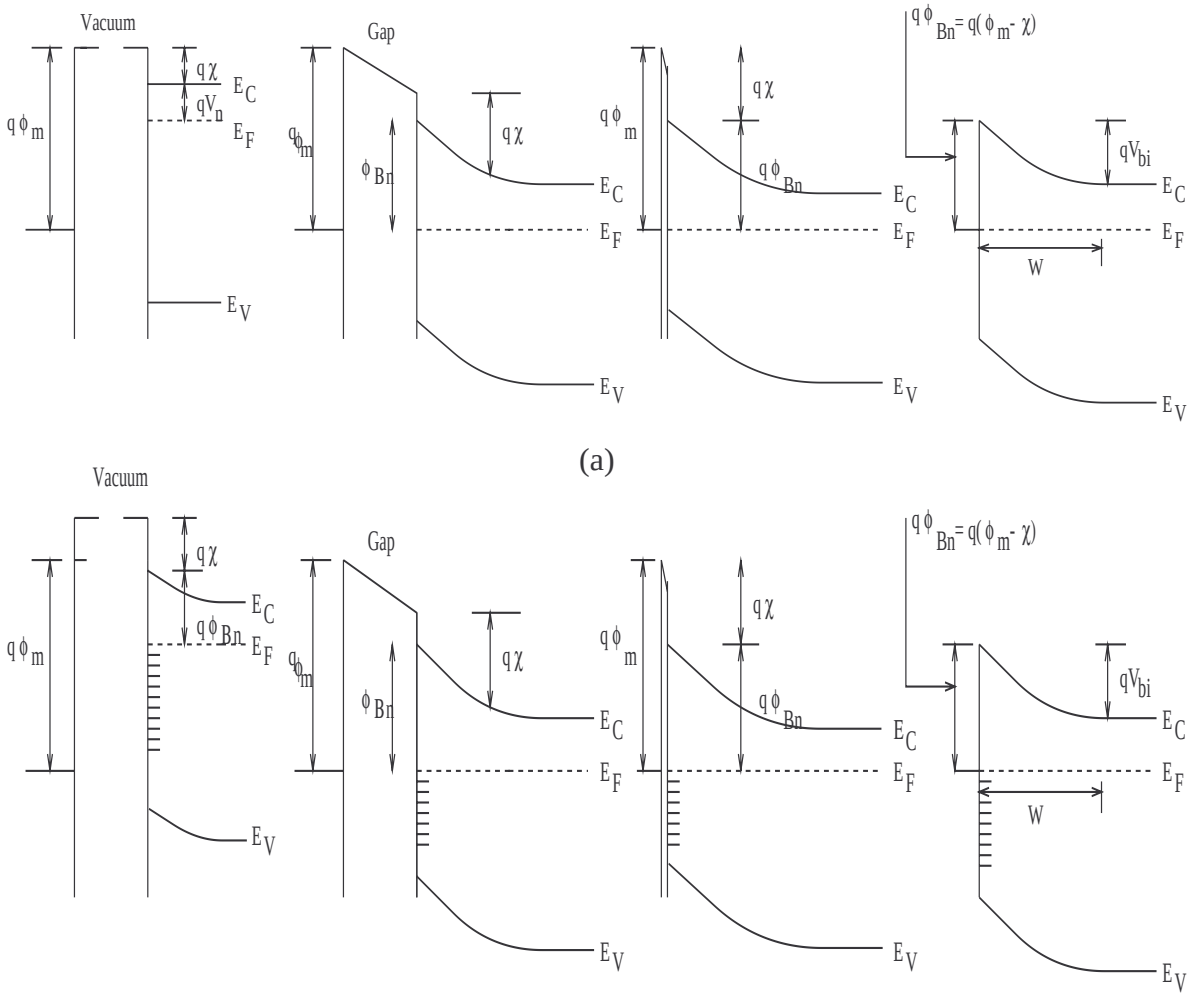


Figure 3 (a) Band Diagram of Metal - Semiconductor in the Ideal Case, (b) With Surface States

Suppose there is a continuous distribution of surface states present at the semiconductor surface characterized by a neutral level φ_0. In the absence of these states, the negative charge on the surface of the metal Q_m must be equal and opposite to the positive charge Q_d due to the uncompensated donors for electrical neutrality. In the presence of these states, the charge neutrality condition is altered to include the effect of

the charges contributed by them, Q_{ss}. The occupancy of the surface states is determined by the fermi level, which is a constant throughout the barrier in the absence of applied bias. For most purposes it is good enough to use an absolute zero approximation in which the states are supposed to be filled upto the fermi level and empty above it. If the neutral level φ_0 happens to be above the fermi level E_f as shown in figure the surface contain a net positive charge and Q_d must therefore be smaller than if the surface states were absent.. This means that the depletion region will be correspondingly reduced, and the amount of band bending will also be decreased.

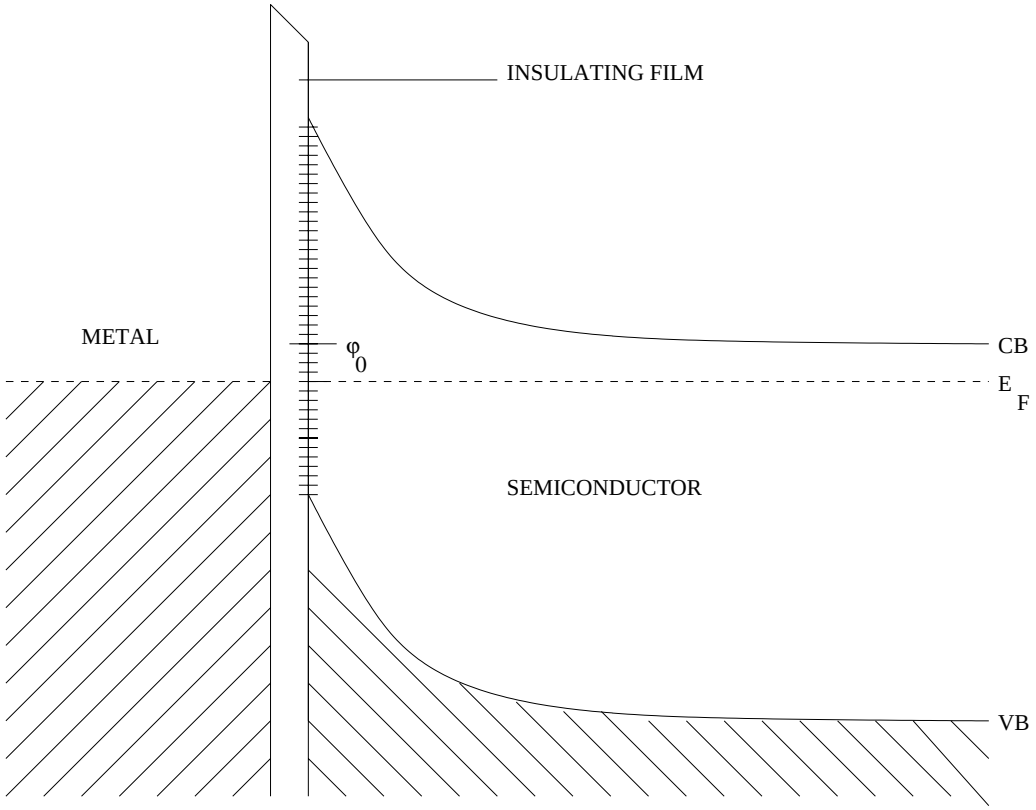


Figure 4 Concept of the Neutral Level

The reduction of φ_b has the effect of pushing φ_0 towards E_f, that is, it tends to reduce the positive charge in the surface states. On the other hand, if φ_0 happens to be below E_f, Q_{ss} is negative and Q_d must be greater than if surface states were absent. This means that w and φb will both be increased and φ_0 will be pulled towards E_f. The surface states therefore behave like a feedback loop, the error signal of which is the deviation of φ_0 from E_f. If the density of the surface states becomes very large, the error signal will be very small and $\varphi_0 \sim E_f$. The barrier height, in this case, is said to be *pinned* by the high density of surface states.

An alternative way of looking at the effect of surface states is to regard them as screening the semiconductor from the electric field, so that the amount of charge in the depletion region is independent of the work function of the metal. Another consequence of the existence of the surface states is that the bands may not be horizontal near the free surface of the semiconductor even when it is not in contact with another solid. If the fermi level does not coincide with the neutral level, there will be a net charge at the surface due to the surface states. This produces an electric field in the semiconductor, which causes bending of the bands. If the surface charge is negative, the bands will bend upward to the surface, and the electron concentration at the surface will be less than that in the interior of the semiconductor. In this situation the surface is said to be depleted. If the charge is positive, the bands will bend downwards, the electron concentration at the surface will exceed that in the interior, and the surface is said to be accumulated. If the density of the surface states is large, the fermi level becomes locked to the neutral level and the work function is almost independent of the donor density in the semiconductor.

2.3.1.3 Current Transport in Metal- Semiconductor Contacts

In contrast to p-n junctions, where the current transport is due to minority carriers, majority carriers mainly contribute to the current transport in metal semiconductor contacts. The various ways in which electrons can be transported across a metal semiconductor junction under forward bias is shown schematically in figure 5. The inverse processes occur under reverse bias. The four mechanisms of transport are [3]:

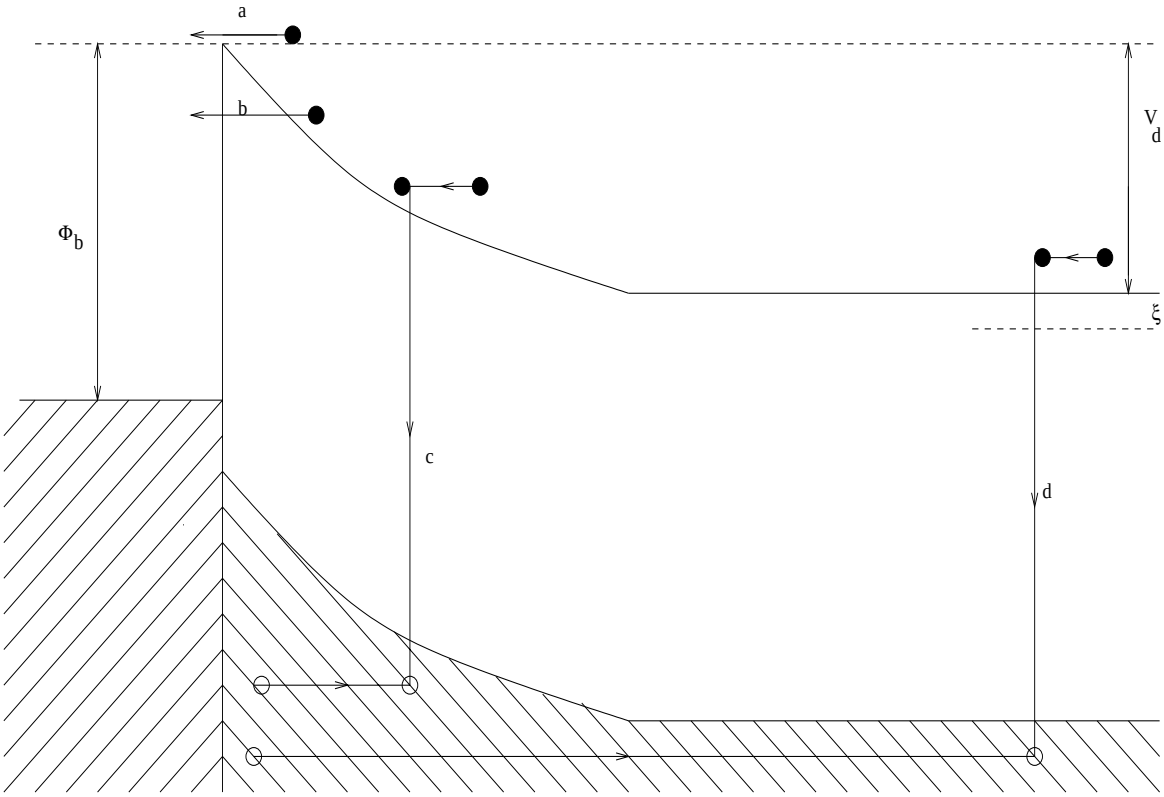


Figure 5 Current Transport Mechanism (Forward Bias) in Metal–Semiconductor Contacts

1) Transport of electrons from the semiconductor into the metal overcoming the potential barrier.
2) Quantum-mechanical tunneling through the barrier.

3) Recombination in the space-charge region.
4) Recombinations in the neutral region, that is, hole injection from the metal to the semiconductor.

2.3.1.3.1 Emission Over the Barrier

The transport of electrons over the barrier is affected by the supply of the same from the interior of the semiconductor. This in turn is affected by the usual mechanisms of drift and diffusion in the electric field of the barrier. In addition, on arriving at the interface the electron emission into the metal is governed by the number of *bloch* states that effectively communicate with the states in the semiconductor. Both of the above processes act in series, and hence the one that provides the maximum impediment to the flow of electrons determines the current. According to the *diffusion* theory the first of these processes control the current flow, whereas the *thermionic emission* theory suggests that the second process is more important. A brief discussion of the basic mechanisms of emission over the barrier is discussed further.

2.3.1.3.1.1 The Diffusion Theory

To obtain the current/voltage characteristic according to the diffusion theory, the current density in the depletion region given by

$$J = qn\mu\xi + qD_e\, dn/dx, \text{ where} \qquad -(1)$$

N is the concentration of electrons in the n-type semiconductor, μ their mobility, De their diffusion constant, ξ the electric field in the barrier, and –q the charge on the electron.

Although this expression is based on the assumption that the mobility and diffusion constant is independent of field, it is frequently used to simplify the analysis.

The quasi fermi level for electrons ζ is given by the expression

$$N = N_c \exp\{-q(E_c - \zeta)/kT\} \quad \text{where} \qquad -(2)$$

Nc is the density of states in the conduction band.

Using Einstein's relationship μ/De = q/kT equation 1 can be written as

$$J = q\mu n \, d\zeta/kT \qquad -(3)$$

The above equation shows that the driving force for electrons is provided by the gradient of ζ. Combining equation 1 and 2 and integrating over thew width of the depletion region yields

$$(J/kT\mu N)\int_0^w \exp(qEc/kT)dx = \exp\{q\zeta(w)/kT\} - \exp\{q\zeta(0)/kT\} \qquad -(4)$$

From the above equation given the value of Ec as a function of x and the values of ζ(w) and ζ(0) for a particular value of bias, the I-V characteristics of the junction can be determined. It is usually convenient to take the fermi level in the metal as reference so that ζ(w) = V. Also the assumption that the concentration of electrons is unchanged on the semiconductor side of the interface makes ζ(0) = 0. This leads to the conclusion that the impediment to the current flow is provided entirely by the drift and diffusion processes in the depletion region. Solving for J in equation we get,

$$J = qN_c\mu\xi_{\max}\exp(-q\varphi_b/kT)\{\exp(qV/kT) - 1\} \qquad -(5)$$

Equation 5 provides the current voltage relationship as predicted by the diffusion theory. It can be seen that the above relationship is quite close to that obtained for an ideal rectifier.

2.3.1.3.1.2 The Thermionic-Emission Theory

In thermionic emission theory the assumption is made that the current-limiting process is the actual transfer of electrons across the interface between the semiconductor and the metal. Here, the effect of drift and diffusion in the depletion region is considered negligible which means that the mobility is infinite. Thus from equation 4 we see that $d\zeta/dx$ is negligibly small so that the quasi fermi level for electrons remains essentially flat throughout the depletion region and coincides with the fermi level in the bulk semiconductor as in the a p-n junction. This implies that the electron concentration on the semiconductor side of the interface is increased by a factor of exp(qV/kT) when a voltage bias V is applied. This situation can be visualized by imagining the existence of a membrane at the interface, which the electrons can penetrate only with difficulty. The membrane keeps the electrons in thermal equilibrium with the bulk of the semiconductor. The current density due to the electrons passing from the semiconductor to the metal is given by

$$J_{sm} = qN_c v \exp\{-q(\varphi_b - V)/kT\}/4 \qquad \text{-(6)}$$

where v is the average thermal velocity of electrons in the semiconductor. In addition there is a flow of electrons from the metal to the semiconductor, which is independent of

the applied bias, as the barrier φ_b remains unchanged. At zero bias these current just balance each other so that

$$J_{ms} = qN_c v \exp(-q\varphi_b / kT)/4 \qquad -(7)$$

Hence, $J = J_{sm} - J_{ms}$

Therefore $J = qN_c v \exp(-q\varphi_b / kT)\{\exp(qV/kT) - 1\}/4$ -(8)

Substituting for Nc gives the I/V characteristics according to the thermionic emission theory as $J = A^* T^2 \exp(-q\varphi b / kY)\{\exp(qV/kT) - 1\}$ -(9)

where A^* is the same as the Richardson constant for thermionic emission.

2.3.1.3.1.3 Effect of Image Force

When an electron approaches a metal, the requirement that the electric field be perpendicular to the surface enables the electric field to be calculated as if there were a positive charge of magnitude q located at the mirror image of the electron with respect to the surface of the metal. Therefore when an electron is at a distance x from the surface of the metal it experiences a force given by

$$F = q^2 / 4\pi\varepsilon_s (2x)^2 \qquad -(10)$$

The effect of the image force is that the barrier, which an electron has to surmount in passing from the metal into the semiconductor, is lowered by an amount $\Delta\varphi_{bi}$, given by

$$\Delta\varphi_{bi} = \{q^3 N_d (\varphi_b - V - \xi - kT/q)/8\pi^2 (\varepsilon_s)^2 N_d\}^{1/4} \qquad -(11)$$

It is however important to discern the effect of image force from the other contributions to φ_b like the work function difference, and surface state charge. The image

force arises from the field due to the particular electron under consideration and is absent if no electron is present in the conduction band near the top of the barrier. Thus barrier height measurements that depend on the movement of conduction electrons or vice versa yield the quantity $\varphi_b - \Delta\varphi_{bi}$. Figure 6 shows the effect of the image force on the bending produced in the conduction and the valence bands. It can be seen that the effect of the image force is to bend the valence band upward near the surface of the metal. Therefore there is no maximum in the top of the valence band as there is in the conduction band, and the energy gap is reduced close to the surface of the metal due to the effect of the image force.

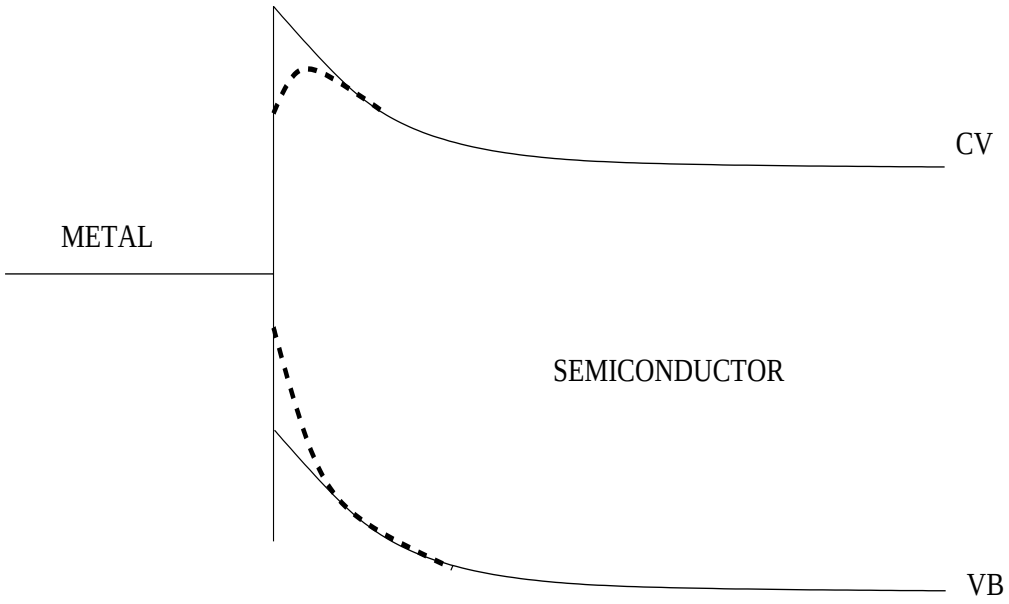


Figure 6 Effect of the Image Force on Barrier Height

2.3.1.3.2 Tunneling Through the Barrier

Electrons with energies less than the barrier height, under certain circumstances, are able to penetrate the barrier by *quantum mechanical tunneling*. In the case of

degenerately doped semiconductors at low temperatures, tunneling of electrons from energies close to the fermi level causes the forward current. This is called *field emission*. If the temperature is raised, the electrons are raised to higher energies thereby rapidly increasing the tunneling probability. This is because the electrons experience is thinner and lower barrier. On the other hand, the number of excited electrons decreases rapidly with increasing energy, and the maximum contribution to the current flow is obtained from electrons, which have energy E_m above the bottom of the conduction band. This is known as *thermionic field emission*. If the temperature is further increased a point is reached in which all the electrons have enough energy to go over the top of the barrier thereby leading to thermionic emission current flow.

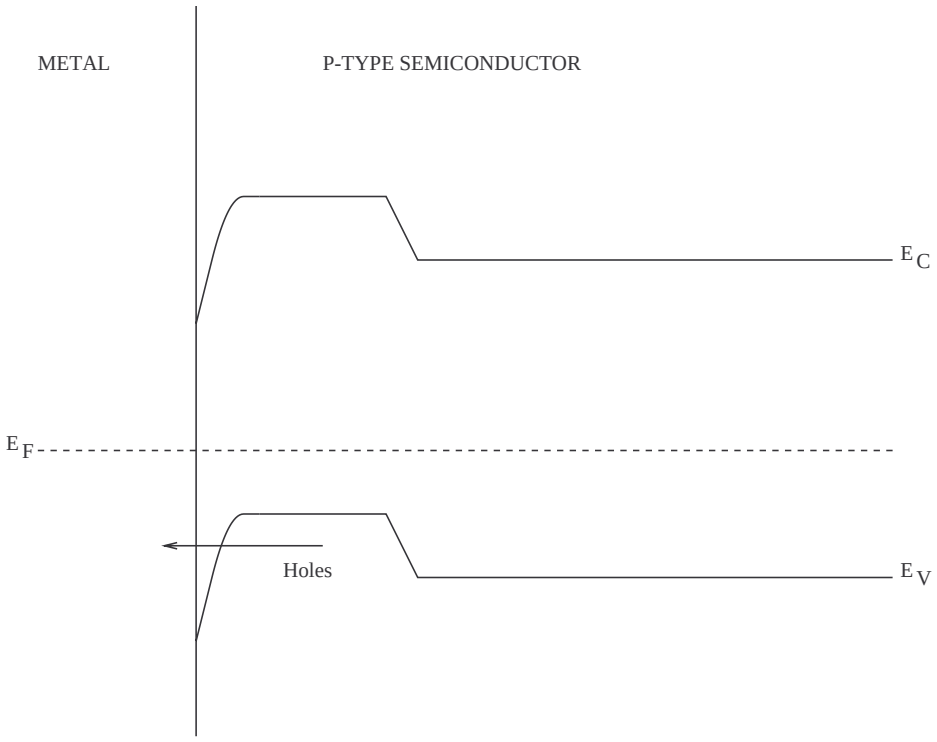


Figure 7 Energy Band Diagram of Metal-Semiconductor Tunneling Contact

One of the most common approaches to obtain near ohmic contacts is to degenerately dope the semiconductor near the contact. This completely saturates the surface states and the donor impurities keep the fermi level within the conduction band. The potential barrier and the depletion layer become so narrow that carriers can tunnel through in both the forward and reverse direction with very little resistance. This process of current transport where the carriers do no overcome the potential barrier across the interface but instead tunnel through it is termed tunneling. Figure 7 shows the energy band diagram of a metal-semiconductor tunneling contact.

2.3.1.3.3 Recombination in the Depletion Region

The recombination of carriers in the space charge region normally occurs due to localized centres. These centres are most effective when their energies lie close to the centre of the gap and progressively reduce towards the conduction and valence bands. The current density due to this recombination center is given approximately by

$$J_r = J_{r0}\{\exp(qV/2kT) - 1\} \qquad \text{-(12)}$$

where $J_{r0} = qn_i w/2\tau_r$. τr is the lifetime in the depletion region.

The total current density is then given by $J = J_{te} + J_r$, or

$$J = J_{t0}\{\exp(qV/kT) - 1\} + J_{r0}\{\exp(qV/2kT) - 1\} \qquad \text{-(13)}$$

For bias voltages greater than 4kT/q the ratio of thermionic to the recombination current is proportional to $\tau_r \exp\{q(E_g - V - 2\varphi_b)/2kT\}$. The ratio J_{te}/J_r increases with τ_r, V, and E_g and decreases with φ_b. Also for low bias voltages the value in the exponential is usually

for n-type semiconductors and the ratio increases with temperature. The contribution to the current due to this phenomenon is thus more pronounced in the case of high barriers, in materials with low lifetime, at low temperatures and low forward bias. Recombination current is a common reason for deviation from ideality in both schottky and p-n junction diodes.

2.3.1.3.4 Hole Injection

The contribution to current due to hole injection occurs when the formation of a schottky barrier causes the region of the semiconductor adjacent to the metal becomes p-type (for an n-type semiconductor) and contains a large density of holes. Some of these holes diffuse into the neutral region of the semiconductor under forward bias, thus giving rise to the injection of holes. In the case of plane contacts like those made using evaporation if we were to assume a flat fermi level in the depletion region the hole density can be written as

$$J_h = qD_h p_0\{\exp(qV/kT) - 1\}/L \qquad \text{-(14)}$$

where p_0 is the equilibrium concentration of holes in the depletion region, D_h and L the diffusion constant of holes in the bulk and thickness of the quasi-neutral region respectively. Assuming thermionic emission theory, the hole injection ratio γh is given by

$$\gamma_h = J_h/(J_h + J_e) \approx J_h/J_e = qD_h n_i^2/N_d LA^{**}T^2 \exp(-q\varphi_b/kT) \qquad \text{-(15)}$$

From the above equation it can be seen that the injection ratio increases with φ_b because of the reduction in J_e, and decreases with N_d because of the decrease in p_0 and the

consequent reduction in J_h. For the usual barrier heights and doping concentrations encountered in silicon diodes the value of the injection ratio is less than 10-4, and thus the hole injection is negligible. However at large forward bias, the electric field in the quasi-neutral region of the semiconductor gives rise to a significant drift component, and for large currents the injection ratio increases linearly with J. The critical current density at which this increase in γh takes place is given by

$$J_c = qD_e N_d / L \qquad \text{-(16)}$$

If the hole injection becomes appreciable at high current densities, the additional electrons enter the neutral region to maintain charge neutrality. This causes the conductivity to increase and hence reduce the series resistance.

2.3.1.4 Schottky Barrier- Reverse Characteristics

According to thermionic-emission theory, the reverse current density of an ideal schottky diode saturates at the value

$$J_0 = A^{**} T^2 \exp(-\varphi_b / kT)$$

There are a number of reasons, however, for a departure from this ideal behavior. Some of the factors are briefly discussed in this section

1) Field dependence of the barrier height: If φ_b is dependent on the barrier height the reverse characteristic of the schottky diode shows incomplete saturation. This is due to the decrease of φ_b with increase in the maximum field, E_{max}, which is the case under reverse bias. The simplest form of barrier lowering is due to the image force. The

barrier lowering introduced is proportional to the applied bias and a plot between lnJ and V_r should be a straight line with the intercept on the ln J giving the J_0. More usually the lowering of the barrier is greater than that predicted due to the image force. The most commom cause for the observed behavior is the presence of an interfacial layer. This is discussed further in the next section.

2) The effect of Tunneling: tunneling through the barrier becomes more significant at lower doping levels in the reverse direction than in the forward direction as the bias voltages involved are much greater. In addition of a moderate reverse bias could make the barrier thin enough for the carriers to tunnel through. As was the case in the forward direction the tunneling could be due to field or thermionic-field emission. Tunneling is the major cause of soft reverse characteristics particularly at the contact edge due to the crowing of the field lines that further accentuate the effect of the image force.
3) Generation in the depletion region: Even if the effect of image force and tunneling were to be minimized using lower doping density the reverse characteristics could still not saturate. This is due to the generation of electron-hole pairs in the depletion region. As discussed earlier, this component is more pronounced in high barrier, low lifetime semiconductors at lower temperatures.

2.3.1.5 The Effect of the Interfacial Layer

Most metal–semiconductor contacts possess a very thin oxide layer between the metal and the semiconductor. Such an insulating layer has three effects

1) Due to the potential drop in the layer the zero-bias barrier height is lower than the case of the ideal diode.
2) The electrons have to tunnel through this layer so that the current for a given bias is reduced.
3) When a bias is applied, part of the voltage is dropped across the oxide so that the barrier height is a function of the applied voltage. This bias dependence alters the shape of the I/V characteristics.

   Another effect of the interface layer is to increase the minority carrier injection ratio under forward bias, as it is controlled by diffusion and essentially unaffected by the interfacial layer. A thicker layer further accentuates this process. In the reverse direction the presence of an interfacial layer causes the effective barrier height to decrease with increasing bias causing no reverse current saturation.

2.3.2 Ohmic Contacts

In a number of cases it is required to obtain contacts, which allow current flow in both the forward and reverse directions. Such contacts have a linear I-V characteristic and are called ohmic contacts. Ideal metal-semiconductor contacts are ohmic when the charge induced in the semiconductor in aligning the fermi levels is provided by majority carriers. For example, consider the same case of a metal -n type semiconductor contact where $\Phi_m < \Phi_s$ .The fermi levels in this case are aligned by the transfer of electrons from the metal to the semiconductor. Thus we find that the semiconductor becomes more n-type. The barrier to electron flow between the metal and the semiconductor is very small and easily

overcome by a small voltage. Unlike the case of schottky barrier no depletion layer develops in the semiconductor, as there is an accumulation of majority carriers in the semiconductor.

2.4 P-N Junctions

P-N junctions are one of the most basic and widely used device structures. Thus a basic understanding of their behavior is essential.

A P-N junction, as the name indicates, is a junction formed between a p-type and a n-type material. P-N junctions are classified into

1) Step junctions

2) Graded junctions

A step junction is one, which has uniform p doping on one side of a sharp junction and uniform n doping on the other side, whereas a graded junction is one, which has a graded impurity profile.

Before the n and p type materials are joined to form the junction, the n material has a large concentration of electrons and fewer holes and the converse is true for holes. Figure 8(a),(b) show the energy bands of each material separately[4].

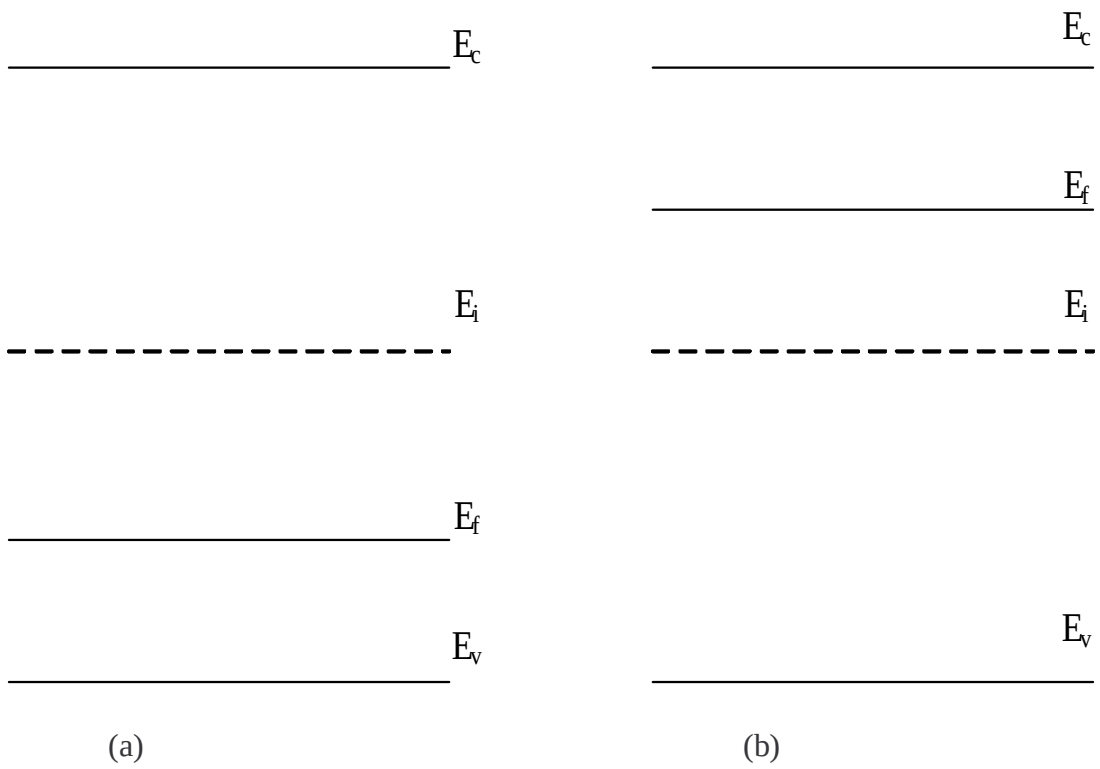


Figure 8 Band Diagrams of (a) P-type, (b) N-type Semiconductors

When these materials are brought together to form the junction diffusion of carriers takes place because of the large concentration gradients. The flow of current as a result of this gradient is called the *diffusion* current. The electrons diffusing from the n to p side leave behind uncompensated donor ions (N_D^+) in the n material, and holes on the other hand leave behind uncompensated acceptors. Thus a positive space charge near the n side and a negative space charge near the p side of the junction develops. This leads to the formation of an electric field E in a direction opposite to the diffusion current for each type of carrier. This field thus creates a drift component of current from n to p opposing the diffusion current. The electric field, builds up to a point where the currents due to

diffusion and drift components cancel each other leading to zero net current at equilibrium. The electric field appears in some region about the junction called the transition, space, or depletion region (as it is depleted of carriers), and the resulting potential difference V_o is called the contact potential. The contact potential separates the bands as shown in figure 9. The valence and conduction bands are higher on the p-side of the junction than on the n-side by an amount qV_0. The separation of the bands at equilibrium is just that required to make the fermi level constant throughout the device.

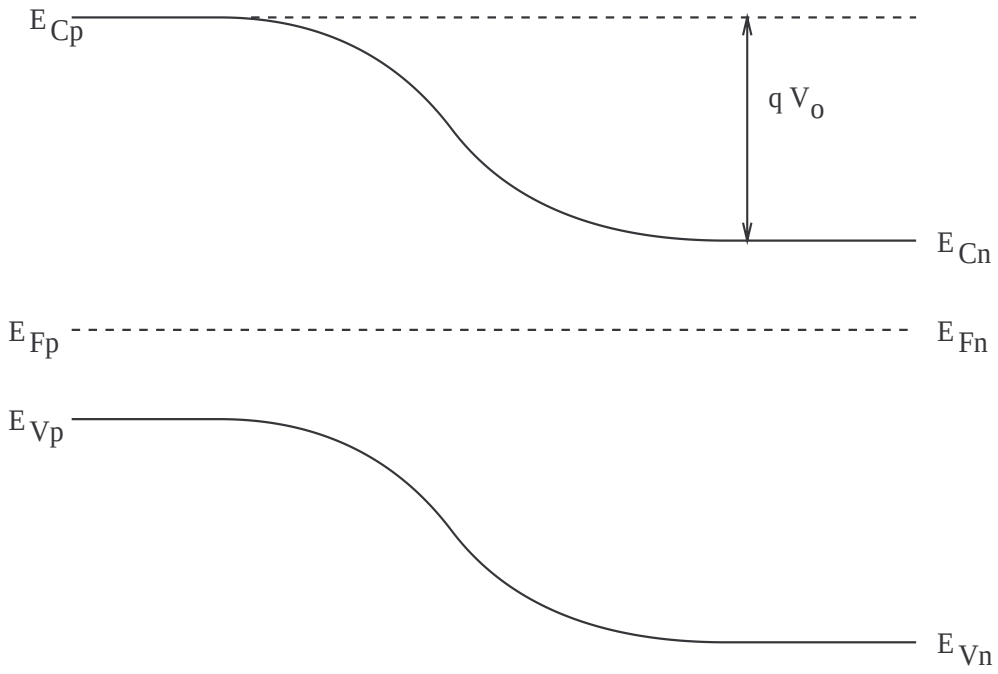


Figure 9 Band-Bending at the Junction

2.4.1 P-N Junction Under Applied Bias

When a p-n junction is subjected to *forward bias*, the electrostatic force of the charge in the battery causes the majority carriers to flow towards the junction. This has the effect of covering up some of the exposed acceptor and donor ions at the edges of the

space charge region. Consequently the strength of the built in field and the gradient of the band-bending reduces as shown in figure 10. Thus the diffusion of the minority carriers exceeds those that tend to drift back in the opposite direction. The fermi level, which is a reflection of this non-equilibrium situation, splits into quasi fermi levels. Assuming that the entire voltage is dropped across the depletion region, the difference in the quasi fermi levels for the quasi-neutral region will equal the bias across the diode, that is,

$$E_{fn} - E_{fp} = qV_{app}. \qquad -(17)$$

The result of the forward bias is that majority carriers flood across the junction, and constitute the dc steady state current seen in a forward biased diode.

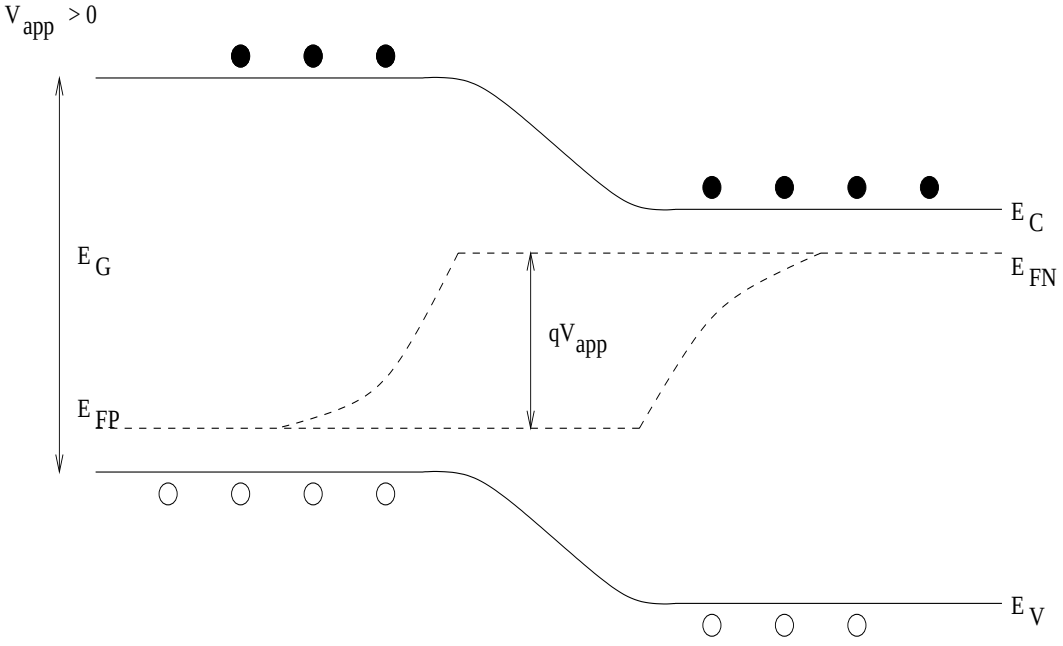


Figure 10 P-N Junction Under Forward Bias

Under *reverse bias* the battery charge causes the majority carriers to move away from the junction thereby causing more ions to be exposed. This causes an increase in the

built-in voltage and the band-bending as shown in figure 11. Consequently there is only minority carrier flow across the junction. The difference in the quasi fermi levels again equals the applied voltage. The current flowing across the junction is minimal and independent of the magnitude of the applied bias. This current is the reverse saturation current observed in a reverse biased p-n diode.

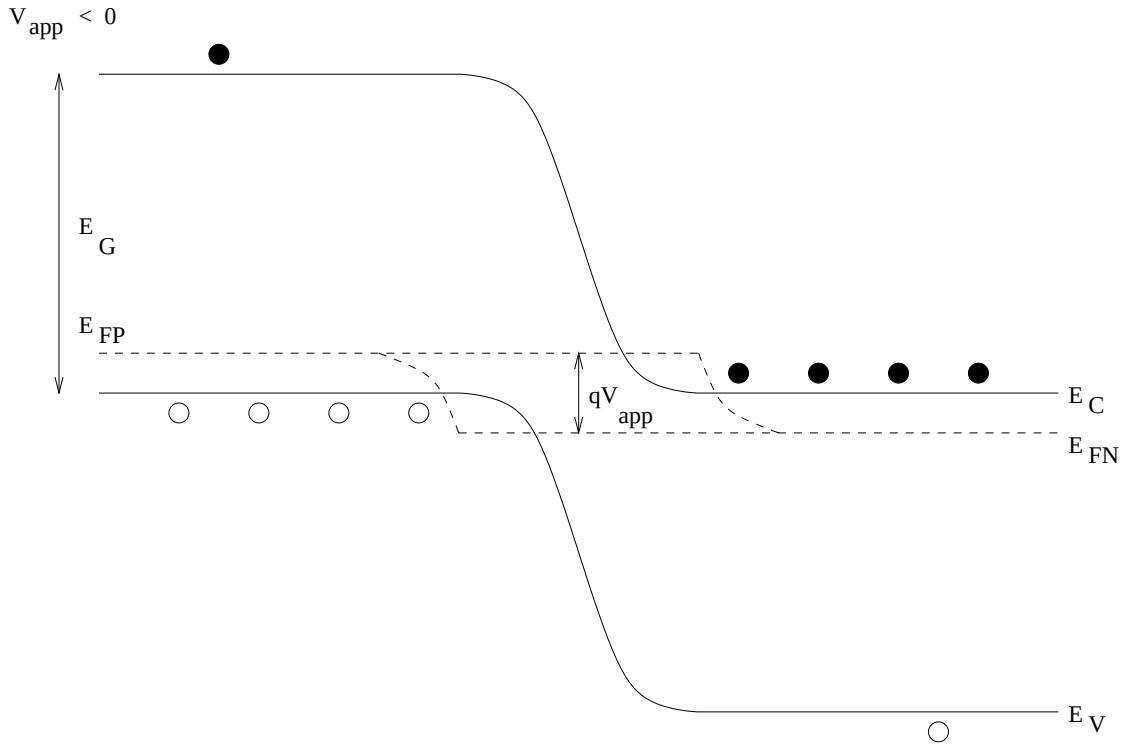


Figure 11 P-N Junction Under Reverse Bias

2.5 Solar Cells

A solar cell is a large-area p-n junction structure designed to convert the sunlight into electric current efficiently. Solar cells use the *photovoltaic effect*, whereby excess photogenerated minority carriers are separated by a junction with a built-in field. Once separated, they arrive as majority carriers on the opposite sides of the junction. This

excess majority carrier concentration is responsible for the creation of voltage across the external circuit. If a load is attached to this circuit a current starts to flow, and useful work is done.

2.5.1 Structure of a Generic Solar Cell

The generic solar cell is a structure consisting of two active layers

1) A thin heavily doped top layer called the *emitter or window* layer.
2) A thick moderately doped bottom layer, called *the base or absorber* with opposite doping.

2.5.2 Fundamental Requirements for Solar Cell

In order to supply power to an external device, a solar cell needs to satisfy three basic requirements [5].

1) The cell must have a volume in which excess electron-hole pairs are generated by the absorption of light.
2) There must be a mechanism to separate the photogenerated carriers
3) The photogenerated carriers must survive long enough to be separated, namely, carrier lifetime should be high.

The first requirement is satisfied by providing a sufficiently long path length, either by having a base thick enough to exceed the absorption length or by the mechanism of light trapping. For a semiconductor sample of arbitrary thickness, the absorption occurs only if

the energy of the incident photon is greater than or equal to the bandgap value, E_g. The expression that relates the wavelength λ, and photon energy E is

$E = hC/\lambda$, where, H is the Planck's constant, and, C= speed of light in vacuum

A p-n junction and the accompanying built-in field meet the second fundamental requirement. The excess electrons and holes, adjacent the junction, in the p and n side respectively are immediately swept by the electric field of the depletion region. However in the case of the solar cell, since the junction is near the surface, most of the light is absorbed in the base. Thus most of the separated charge consists of electrons from the base.

The final requirements is satisfied by the use of moderately doped materials with low crystallographic defect densities, which causes the diffusion length of excess electrons to be large in the base. In order to obtain higher open circuit voltages (discussed in the next section) it is desirable to have a higher doping in the base. This is because for higher doping densities a strong built-in field is produced and thus provides an enhanced gradient for excess carriers. However the lifetime of the carrier reduces with doping. Hence a trade-off between increased built-in field and increase lifetime in the bulk is usually made for optimum performance.

Thus, a solar cell uses its thick base to absorb light and produce excess electrons, which diffuse over to the depletion region. The field in this region causes them to be swept into the emitter where they are the majority carriers and thus feel little concentration gradient. However the electrons repel each other due to coloumbic force that causes them to be removed at the front contact of the cell. It is this photo generated excess charge, and

not the built-in voltage that produces a voltage across the external circuit. The excess holes in the emitter behave analogously to the excess electrons in the base. However since the junction is shallow, most of the light reaches the base and few electron-hole pairs (e-h) are created in the base. The blue end of the spectrum produces the e-h pairs, which has a short absorption length. In addition, due to the greater doping in the emitter the diffusion length of holes is greatly reduced.

From the discussion above, it seems that the current in a closed circuit solar cell is the photogenerated current. However it is important to consider the effect of the diode current when no light is present, or the dark current. The presence of the excess majority carriers at the edges of the depletion region has the effect of forward biasing the p-n junction. This in turn causes the potential barrier to reduce, thereby aiding the diffusion of majority carriers across the junction. Thus it can be seen that the separated photo carriers cause a current that opposes the photogenerated current. This current equals the current generated by the forward biased diode in the dark. The dark current is hence a parasitic component that needs to be minimized to obtain the maximum current from the cell. This is usually achieved by increasing the minority carrier diffusion length in the base or reducing the base thickness.

2.5.3 Parameters of a Solar Cell

Several parameters are used to characterize solar cells. In this section we will briefly review some of these parameters and how they influence the performance of the device[6]. Figure 12 shows the I-V characteristics of a solar cell in the dark and under

illumination. The product of voltage and current in the fourth quadrant is negative indicating that the cell puts out power, and this is the region of interest in solar cells. One of the parameters is the short circuit current I_{sc} which is defined as the current flowing in the circuit when the load is shorted.

The open circuit voltage V_{oc} another important parameter, is the voltage output of the cell when the attached load is infinite and is given by the relation

$$V_{oc} = A_o(kT/q)(I_{sc}/I_o + 1) \qquad (18)$$

where I_o is the reverse saturation current or the dark current at the junction.

The expression for the total current is,

$$I = I_0(e^{qV/AkT} - 1) - I_L \qquad -(19)$$

where I_L is the light generated current.

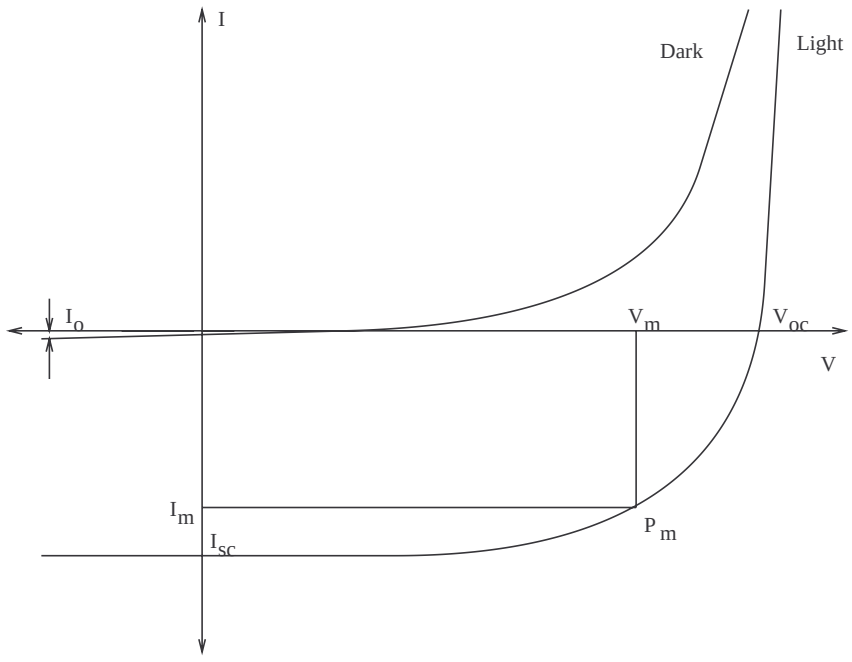


Figure 12 I-V Curve of the Solar Cell in Dark and under Illumination

Both I_o and A_o provide important information on the predominant current transport mechanism in a device. There are a number of ways of obtaining these parameters, although the most consistent method involves their determination using the dark J-V curves. The slope of the J-V curve gives the A_o, whereas the y-intercept gives the J_o. They are usually considered together as there is great deal of correlation between the two parameters. It is desirable that J_o be as low as possible, so that higher voltages are required for the dark current to equal the light generated current. This increases the V_{oc} of the devices. A lower value of A_o reduces V_{oc} but helps increase the fill factors of devices. The discussion of A_o and J_o is more complex and needs a more careful analysis. Oman et. al analyzes these parameters and their effect on cell behavior in greater detail[6]. We shall conclude our discussion here as it is beyond the scope of this research.

In Figure 13 an inverted I-V characteristics of a solar cell in the fourth quadrant is shown.

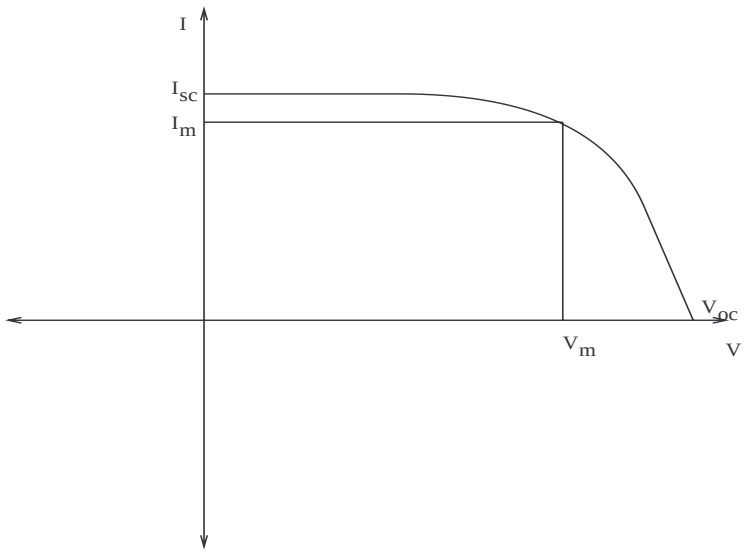


Figure 13 Inverted I-V Curve

I_{sc} and V_{oc} are the short circuit current and the open circuit voltage and I_m and V_m are the current and voltage corresponding to the maximum power point. This is the point where maximum power can be generated by the device.

Another parameter of interest is the Fill factor given by the relation,

$$FF = V_m I_m / V_{oc} I_{sc} \qquad -(20)$$

The photovoltaic conversion efficiency is another important parameter. It is a measure of the amount of light energy that is converted into electrical energy and is given by

$$\eta = P_m/P_{in} = FF \times I_{sc} \times V_{oc} / P_{in} \qquad -(21)$$

where P_m is the area of the maximum power rectangle, and P_{in} is the incident power

2.5.4 Series and Shunt Resistance

Although it is desirable to have zero series resistance and infinite shunt resistance,

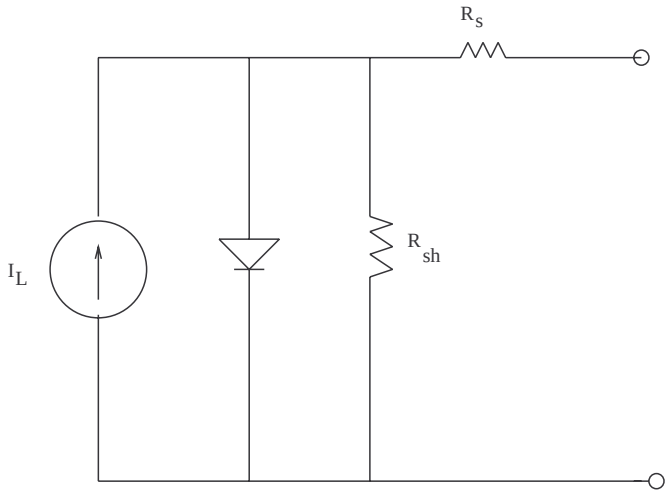


Figure 14 Equivalent Circuit of a Solar Cell

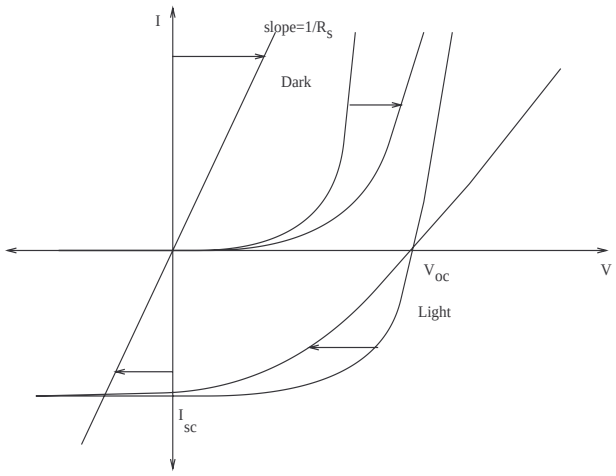
all the practical solar cells are characterized by a finite series and shunt resistance. Figure 14 shows the equivalent circuit of a typical solar cell with a current source shunted by diode and shunt resistance R_{sh}, all in series with a resistance in series R_s, to produce a terminal voltage V and current I.

The total current taking the series and shun resistances into account is given by

$$I = I_o[\exp(V\text{-}IR_s/AkT) - 1] - I_L + (V\text{-}IR_s)/R_p \qquad \text{-(22)}$$

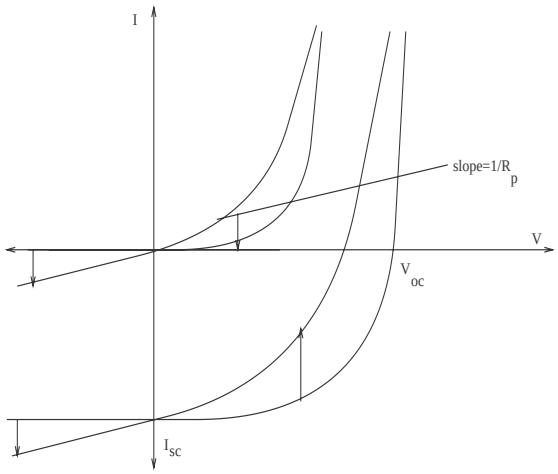
2.5.4.1 Effect of R_s and R_p

Figures 15a,b[3] show the effect of the series and shunt resistance on the I-V characteristic using graphical construction.



(a)

Figure 15 (a) Effect of Series Resistance, (b) Effect of Shunt Resistance



(b)

Figure 15 Continued

The effect of R_s is illustrated by the graphical addition of the I-V curve of the cell and the resistance characteristic with slope 1/ R_s .It can be seen that the V_{oc} remains unaffected by R_s and I_{sc} is changed very little unless R_s is very large, in which case the cell characteristic approaches $1/R_s$.

Similarly the effect of R_p can be obtained by the addition at constant voltage, of the zero resistance I-V curve and $1/R_p$. In this case I_{sc} is unaltered whereas V_{oc} may be changed slightly.

Another parameter affected by R_s and R_p is the FF, which decreases with increase in R_s and decrease in R_p

2.5.5 Heterojunction Solar Cells

Heterojunction solar cells in contrast to the homojunction solar cells are fabricated using two different semiconductors with different bandgaps. The band diagram of a typical heterojunction in thermal equilibrium is shown in figure 11.

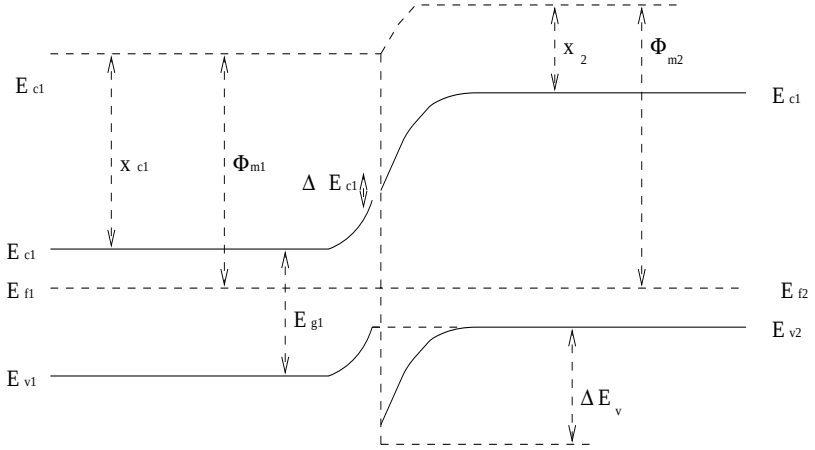


Figure 16 P-N Heterojunction

Light, with energy less than Eg1 but greater than Eg2 passes through the first semiconductor. The first semiconductor acts as a window, the second semiconductor, the absorber. Carriers generated in the depletion region and within a diffusion length of the junction are collected and contribute to the photocurrent. In heterojunctions, the use of two chemically different materials introduces certain problems not encountered in homojunctions such as chemical compatibility and stability, reproducibility of the physical and chemical interface, and the lattice compatibility at the metallurgical junction. Despite the problems mentioned above, the use of heterojunctions has a few attractive features.

Firstly, the heterojunctions allow the use of semiconductors that can only be doped either p-type or n-type and have attractive properties like better match to the solar spectrum, direct band gap or better-cost considerations. Secondly, heterojunctions of the window-absorber form can be used to form structures that shield carriers from the top surface or back surface recombination sinks. Thirdly, the heterojunction solar cell is capable of producing more open circuit voltage than a homojunction even though the built-in voltage is the same in both the structures.

Unlike the situation in homojunctions the carrier transport properties are controlled by interface phenomena. The current transport in the depletion region is attributed to recombination, tunneling or a combination of both tunneling and recombination through the energy levels produced by these interface states. In the next section a detailed account of the various models describing heterojunction theory is discussed.

2.5.5.1 The Anderson Model

The Anderson theory forms the basis for most other heterojunction theories. In this theory discontinuities in material properties like εs,χ, and Eg across an abrupt metallurgical interface are introduced to the Shockley diode theory. The result of these modifications when introduced during the junction formation between two semiconductors results in the band diagram shown in figure 16. The basic assumption of the this model is that no interface states are present and that the current transport is through the injection into the quasi-neutral region or generation/recombination in the depletion layer, which is

seldom the case with typical heterojunctions. The relationship between the various quantities is given by

$$\Delta Ec = (\chi 1-\chi 2)q, \qquad \Delta Ev = (\chi 2-\chi 1)q + Eg2-Eg1 \qquad -(23)$$

$$qV_d = qV_{d1} + qV_{d2} = Eg1-\delta n-\delta p+\Delta Ec \qquad -(24)$$

$$V = V1+V2, \qquad -(25)$$

$$V_{d2}/V_{d1} = V2/V1 = (V_{d2}-V2)/(V_{d1}-V1) \qquad -(26)$$

Here V_{d1} and V_{d2} are the diffusion voltages and V1 and V2 is the portion of the applied voltage dropped on either side of the junction. The heterojunction of figure which represents the usual configuration for a CdS/CdTe solar cell, requires Eg2>Eg1 to maximize the bandgap window so that in most cases the transport of one of the carrier types across the metallurgical junction dominate. Thus the hole transport across the interface to recombine in the n-QNR is negligible with respect to the electron current because of the large barrier to the holes. In addition, the photogeneration in the window material can be usually neglected because its thickness is much greater than the diffusion length so that the hole transport to the left can be neglected for the case in figure. For diffusion dominated transport the I-V relationship is similar to a homojunction and given by

$$J \cong q(D_{n1}/L_{n1})(n_i^{\,2}/N_{A1})[\exp(qV/kT)-1] \qquad -(27)$$

Where V is the applied bias, $V= V_1+V_2$. From the above equation it is clear that the magnitude of ΔE_c does not affect the transport until the flat-band condition $V= V_{d1}+V_{d2}$.

The Anderson model although predicts the bands quite successfully, although the J-V relationship obtained using this model is quite different from the measured values. Thus the model needs to be modified. Another drawback of the Anderson model is the assumption of a perfectly abrupt metallurgical junction. This assumption is not suitable for practical junctions since most junctions, by virtue of being fabricated at high temperatures, are graded junctions due to the intermixing between the constituent materials. This typically causes some of the spikes observed in the conduction or valence band (conduction band in our case) to be smeared to the point where it no longer affects or impedes the carrier flow.

Another major modification that is required to model heterojunction theory is to take account of the effect of interface states. A brief description of the nature of interface states is discussed in the next section.

2.5.5.2 The Effect of Interface States

Interface defects arise due to the lattice mismatch between the materials that form the heterojunction, and from the impurities or defects introduced during the fabrication of the junction. The difference in the lattice constant causes formation of dangling bonds, which may be electrically active, thereby serving as sites for impurity segregation. The lattice mismatch also produces lattice strain, which beyond a certain critical value causes dislocations to propagate away from the interface along the growth direction.

The presence of a large number of interface states (electrically active) provides two mechanisms in heterojunctions.

1) The charge stored in the states distorts the band profile, raising ore lowering the conduction bands at the interface with respect to the equilibrium fermi level.

2) These states provide a large density of recombination centers needed to explain the high J_0 observed in devices. This behavior can be quantified by an effective interface recombination velocity S_I

2.5.5.3 Models of Heterojunction Transport

A number of different models have been advanced for HJ transport in various types of junctions differing mainly in the dominant or limiting step in the transport route. Parallel routes in general do not react with each other and the resulting current is the sum of the individual components. In a series combination on the other hand is characterized by the limiting step. The different transport models are described in this section.

2.5.5.3.1 Injection and Diffusion in the QNR

This model is very similar to that encountered in the case of homojunction. The assumptions used in this model are similar to those in the Anderson's model. These include requirement of junction abruptness, complete equilibrium across the depletion layer, and no recombination in the depletion region. Thus the current-voltage relationship is similarly written as

$$J \cong q(D_{n1}/L_{n1})[N_{c1}N_{d1}/N_{c2}]\exp(-qV_b/kT)[\exp(qV/kT)-1] \qquad \text{-(28)}$$

where $V_b = V_{d1} + V_{d2} - \Delta E_c$

Although this model provides a basic framework for the current transport it is quite inadequate in the case of modeling heterojunction transport due to the assumptions made in the anderson model. Typically the model predicts Jo values orders of magnitude lower than that observed experimentally.

2.5.5.3.2 Recombination/Generation in the Depletion Layer

In the typical HJ solar cell, recombination/generation is expected to be largely confined to the side of the depletion layer in the smaller band-gap component, because of the large barrier to minority injection into the large band-gap component. Here again the J-V relationship can be obtained from the analysis of the homojunction provided the position of maximum recombination lies well inside the depletion layer of the p-type material. In CdS/CdTe solar cells this is usually the case and the maximum lies well within the p-type CdTe region.

The treatment of the R/G transport mechanism can be simplified by assuming that the quasi-fermi levels are constant in the depletion region. Based on the Shockley-Read recombination theory, maximum recombination occurs when the intrinsic level lies approximately halfway between the electron and hole quasi-fermi levels, and rapidly decreases on either side of this level. In the case of forward bias this region of

recombination is confined over a small area of the depletion region and the current contribution due to this is given by

$$J_{rg}{}^{+} \cong n_i W_D kT / 2(V_D - V)\tau_{n0}[\exp(qV / 2kT) - 1] \qquad \text{-(29)}$$

In contrast to the case of forward bias the maximum rate in reverse bias increases in width for increasing bias voltage, finally becoming constant over almost the whole depletion region. The resulting current considering the effect of the change in Efn and Efp is given by

$$J_{rg}{}^{-} = -qW_D(V)n_i(2(\tau_{n0}\tau_{p0})^{1/2}\cosh\{[E_r - E_i / kT] + \ln(\tau_{n0} / \tau_{p0})^{1/2}\})^{-1} \qquad \text{-(30)}$$

The above expressions are derived for the case of recombination centers with uniform distributions and located at a certain energy level in the band-gap. However in order to explain the I-V curves obtained more accurately it is necessary to include the effects of several intercommunicating sets of recombination centers

2.5.5.3.3 Direct Recombination through Interface States

Recombination through interface states is an important route of transport in many heterojunctions due to the lattice mismatch encountered in the junction forming materials. In this model the heterojunction is split into two schottky diodes connected back to back

by a layer of interface states where recombination is strong. The expression for the J-V relationship based on this model is given by

$$J = J_0 \exp(-\Delta E / kT)[\exp(qV / AkT) - 1] \qquad \text{-(31)}$$

where J_0 and A are slow varying functions of T and V, and 1<A<2. This model fall short in that it does not explain the temperature –independent slopes of the logJ versus V curves seen in many heterojunctions.

2.5.5.3.4 Transport by Interface Recombination

The difference between the previous mechanism of transport and the transport bt interface recombination is in the limiting step of the process. While in the previous case it was the thermionic emission over the barrier that limited the curent transport, in the present case the limiting step is interfacial recombination characterized by a recombination velocity S_i. The J-V relationship is given by the equation

$$J(V) \cong qS_i(n_n - n_{n0}) = qS_i N_D \exp(-qV_d kT)[\exp(qV / kT) - 1] \qquad \text{-(32)}$$

2.5.5.3.5 Tunneling

The lack of dependence of the J-V curve with temperature suggests that tunneling through the barrier dominates the current transport in heterojunctions. The probability of this mode of transport increases with the reduction in the thickness of the barrier.

Tunneling can be either intraband or interband tunneling. In the former case the tunneling through the conduction band spike is the limiting step for injection into the p-type. In interband tunneling through states in the depletion layer is the limiting step. A further development of tunneling limited transport is the stepwise tunneling and recombination through a staircase of closely spaced states in the interface region.

For a more detailed analysis of the various models of heterojunction transport the reader is referred to ref[7]. In the next chapter a detailed overview of the properties of CdTe that affect contact formation is discussed. In addition, a detailed literature review of the various ohmic and pseudo-ohmic contacts fabricated on p-CdTe is presented.

Chapter 3

CdS/CdTe SOLAR CELL

The CdS/CdTe heterojunction is one of the most significant candidates for photovoltaic conversion of solar energy. In this chapter a brief discussion of the properties of these materials is presented.

3.1 Cadmium Sulfide

CdS, one of the most widely used materials for window layers in solar cells, crystallizes into the zinc blende (cubic) or the wurtzite (hexagonal) structure [8]. In the hexagonal close packed structure with alternating Cd and S atoms, each Cd atom is surrounded by four nearest neighbor S atoms. The structure is shown in figure 17.

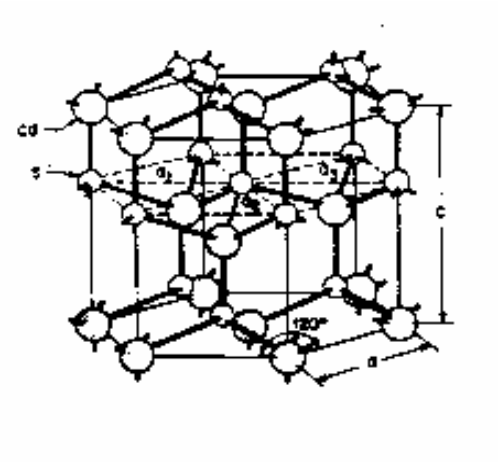


Figure 17 Hexagonal Structure of CdS

CdS is a II-VI semiconductor with a bandgap of 2.42eV at 300K. Unlike elemental semiconductors like Si and Ge the doping of II-VI compounds like CdS, is more complex. This is due to predominance of self-compensation, which is caused by certain native defects like point defect and dislocations. Point defects can be vacancies or interstitial atoms. The conductivity of CdS, as in the case of other II-VI compounds, is influenced by vacancies and defects. The sulfur vacancies act as singly ionized donors [9] and contribute to the n-type conductivity. As-deposited CdS is highly resistive (of the order of 10^6 Ω cm [10]), which can be reduced by annealing in hydrogen (increases sulfur vacancies) and dopant incorporation. The optical properties of CdS make it an ideal choice for window layers in thin film solar cells. It absorbs light below a wavelength of about 510 nm(a very high absorption coefficient of 10^5 cm^{-1}), and thus a large portion of the visible solar spectrum is transmitted. The transmission of light in the blue region (<510nm) of the spectrum depends on its thickness.

CdS has been a very versatile window layer, in that it has been the junction partner in a number of solar cells, using Cu_2S, InP, CIS, CdTe, etc. Of these, the CdS/CdTe heterojunction has aroused the maximum interest.

There are several cost-effective techniques used for the preparation of CdS like, chemical bath deposition (CBD), close-spaced sublimation (CSS), screen printing and sputtering. The best results have been obtained with the CBD process, although the use of this method for large-scale production is questionable due to the problems encountered with the disposal of Cd laden wastes. Recent results with cells made using CdS made by CSS technique have proved to be as effective with the added advantage of being more industrially viable.

3.2 Cadmium Telluride

Cadmium telluride, a II-VI semiconductor crystallizes in the zinc-blende structure as shown in figure 18.

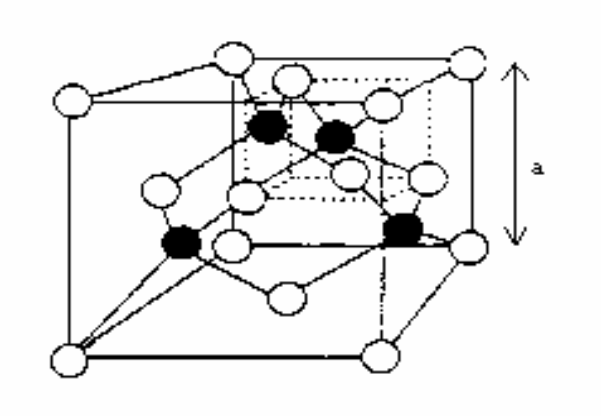


Figure 18 CdTe-Zinc Blende Structure

It has a lattice parameter of 6.48 Å [2]. It is the only II-VI semiconductor that can be easily doped n or p type. CdTe is characterized by the presence of a number of native effects, which act as donors or acceptors. In addition these defects form complexes with the dopant and thus make control of CdTe properties difficult. The electron and hole mobilities are 1100 and 80 $cm^2v^{-1}s^{-1}$ for high purity single crystals [8]. Polycrystalline CdTe can be grown using a number of low cost fabrication techniques like sputtering, electrodeposition, screen printing, chemical vapor deposition (MOCVD), and close-spaced sublimation.

As has been shown in earlier studies of the solar spectrum and semiconductor characteristics the conversion efficiencies of solar cells is dependent on the bandgap and is a maximum for a bandgap of 1.5 eV. CdTe with a direct bandgap of 1.44 eV at room temperature is very close to this condition. Being a direct bandgap material, it has a high

absorption coefficient of $5*10^4$ cm^{-1} for photon energies greater than its bandgap. Thus a thickness of 1-2 μm is enough to absorb 99% of the above bandgap light. This property of CdTe makes it less suitable for homojunction solar cells, although the heterojunction solar cells are capable of high efficiencies.

During recent years p-CdTe has gained a great deal of importance as solar cell absorbers in heterojunction solar cells. The best heterojunction partner for CdTe is CdS and very high efficiencies have been achieved using this structure. This is primarily due to the compatability with CdS properties (lattice mismatch of 9.7%) [11] as compared to other window layers. One of the limitations of CdTe is the difficulty of obtaining ohmic contacts. The discussion of ohmic contacts to CdTe is presented later (chapter 4).

3.3 CdS/CdTe Heterojunction

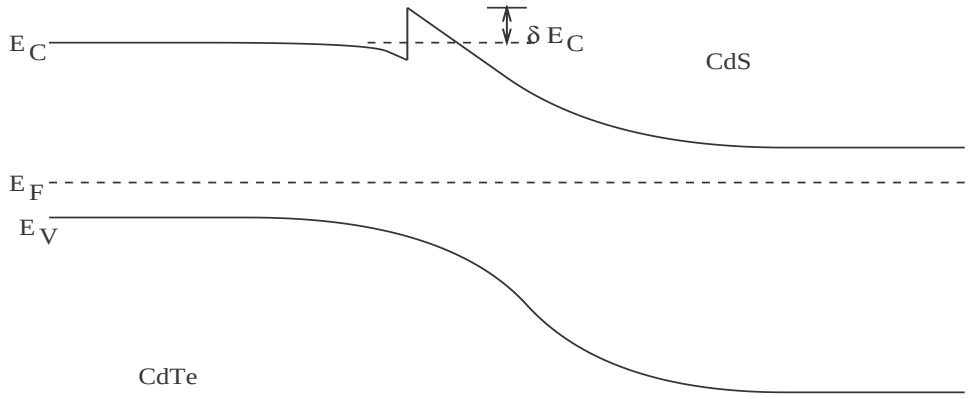


Figure 19 Spike at the CdS/CdTe Heterojunction

Figure 19 shows the band diagram of a nCdS/ pCdTe heterojunction. The spike at the junction is due to the high electron affinity of CdS, which causes this discontinuity.

However this discontinuity is smoothened out due to the interdiffusion of CdS and CdTe during the formation of the heterojunction. Some of the properties of CdS and CdTe are listed in table 2[12].

Table 2 Properties of CdS and CdTe

	CdS	**CdTe**
Bandgap (eV)	2.42	1.44
Electron Affinity (eV)	4.5	4.2
Dielectric Constant	9.7	7.2
Mobility **(**Electrons) at room T (cm /Vs)	340	1200
Mobility **(**Holes) at room T (cm /Vs)	15	50
Refractive Index	2.33	2.5
Lattice Parameters (Å)	5.832	6.447

CHAPTER 4

CdTe BACK CONTACT TECHNOLOGY

In chapter 2 a brief review of the basic physics behind metal-semiconductors junction was discussed. In practical contacts however, the situation is not very straightforward and usually involves a more complex process. In this chapter a detailed review of contacts pertaining to p-CdTe is presented.

4.1 The Contact Problem

The formation of stable, reproducible, low resistance contact to p-CdTe is one of the major problems in the fabrication of efficient solar cells. The reason for this is discussed in the succeeding sections.

1) Work function of CdTe

2) Doping of CdTe

4.1.1 High Work Function of CdTe

A barrier free contact to a p type semiconductor, as discussed in chapter 2, is obtained when the work function of the metal is greater than that of the semiconductor. The electron affinity of CdTe has been found to be about 4.5eV and the distance between

the conduction band and the fermi level, in the case of p-CdTe, can be estimated to be 1.38-1.48 eV [13]. Thus the value of the work function is about 5.9eV. In Table 3 some of the most commonly used metal for contacts are presented [14].

Table 3 Metals - Work Functions

Metal	Work function (eV)
Mo	4.2
Ag	4.7
Al	4.4
Au	5.1
Co	5.0
Cu	4.65
Ni	5.15
Pd	5.1
Pt	5.6

As is evident, no metal presents a value, that can help reduce the barrier height sufficiently to even make a quasi-ohmic contact, and thus most of the contacts to p-CdTe are rectifying. Metals like gold, nickel, carbon (graphite), and platinum have been used, although the contact resistivity is either not low enough or the stability of the contact for solar cell purposes is questionable. The approaches used to overcome this limitation are discussed further.

4.1.2 The Doping Problem

The inability of obtaining low resistivity CdTe is another limitation. The problem of satisfactory doping limits the maximum V_{oc} obtainable from the device. Other advantages of a higher carrier density are reduction in photoconductivity and in atmospheric insensitivity. This in turn improves the time stability of electronic properties.

CdTe being a defect semiconductor, the carrier density is controlled to a large extent by native defects, with or without extrinsic doping. Native defects act as donors and acceptors with cadmium and tellurium vacancies or interstitials acting as acceptors and donors respectively. Extrinsic dopants influence the materials electrical characteristics if they are present as single ionized impurities or as part of complexes with a native defect. A prominent example is the V_{cd}-Cl_{Te} complex, identified as an acceptor. In single crystalline CdTe(SC) doping concentrations in the range of 10^{17} - 10^{18} cm^{-3} have been obtained by the indiffusion of both p-type and n-type impurities. By incorporating group III materials like indium, gallium, and aluminum during crystal growth, donor densities of $2*10^{18}$ cm^{-3} have been obtained, depending on P_{cd}[15]. Group V elements like phosphorous and arsenic can be readily incorporated during crystal growth and acceptor concentration of $6*10^{17}$ cm^{-3} have been realized. Group IA elements also provide shallow acceptor levels in SC CdTe. Introduction of sodium and lithium has yielded carrier densities of upto 10^{19} cm^{-3} by incorporation during growth or during subsequent incorporation by diffusion. Group IB metals (noble metals) like gold, silver, and copper have also been successfully used to dope CdTe, although their activity is quite complex.

Carrier densities higher than 10^{17} cm^{-3} is usually adequate to produce pseudo ohmic contacts with minor R_c losses on single crystalline p-CdTe based cells, but the problem of doping is more severe in the case of a poly-crystalline materials (PC). In a PC material, excessive series resistance arises from potential barriers both at the grain boundaries and at the p-type ohmic contact. The heights of these barriers are controlled not only by the impurity and dangling bond states, but also by the carrier density in the bulk adjacent to the barriers. In addition the doping control is difficult because, the oppositely charged grain boundary states effectively compensate the dopant. For large grain boundary potential barriers the effective carrier density is substantially reduced by the presence of grain boundary depletion regions and the effective mobility is strongly reduced by the grain boundary barriers [15]. The surface recombination velocity, a very important parameter in thin films, reduces with the reduction in the barrier height, indicating that sufficient doping is needed for fabricating cells with high conversion efficiencies.

Owing to the above reasons, very limited success has been obtained in doping PC CdTe p- type. Attempts at doping during growth have been limited to carrier densities of 10^{15}-10^{16} cm^{-3} (intrinsic) [16]. Chu et al reported the introduction of phosphorous and arsenic during MOCVD giving a p-type resistivity of 200Ω cm and carrier densities of 10^{16} cm^{-3} depending on controlled stoichiometry [17]. The use of antimony during growth has also been unsuccessful due to lack of Sb incorporation by substitution. High Sb amounts also lead to an abrupt reduction in resistivity (high conductivity) due to antimony precipitation. Element like Li, Cu, Hg and gold have been used with some

success but are questionable for use in CdTe for devices. Previous work done in doping CdTe p-type, at USF, by introduction of As in the form of AsH_3 by MOCVD were very ineffective due to compensation effects and complex formation [18].

From the problems discussed above it is evident that the formation of ohmic contacts to CdTe tends to be more of an art than science.

4.2 Contact Approaches

Most of the common approaches used to form ohmic or pseudo ohmic contacts fall under four general methods:

1) Utilization of a contact material with the proper work function, to provide a low barrier height at the contact,
2) Heavily doping the semiconductor adjacent to the contact to promote tunneling,
3) Adding recombination centers to the semiconductor adjacent to the contact, and/or
4) Changing the fermi level pinning at the metal-semiconductor interface.

Of the methods mentioned above, not all have proved suitable for CdTe. In method 3, recombination centers are created within the junction barrier to promote multi-step tunneling. This is done by hitting the junction with a short and intense electrical discharge. The resulting imperfections however cause a decrease in the carrier density. Thus there is no appreciable reduction in R_c.

The fourth alternative of altering the fermi level pinning at the surface is a fruitful approach and liquid junctions can provide such an unpinned surface to which ohmic contacts can be made. The use of this approach is unfortunately useful only for laboratory characterization and its ultimate stability is open for question. Thus most of the contacts are formed predominantly by the first two methods.

As no metal has a work function as high as CdTe, a variation of the first method is used. This involves interposing a layer of another semiconductor at the contact, which forms a pseudo ohmic contact to the metal more easily. The important consideration is the match required in the electron affinities of CdTe and the interposed semiconductor. In general most contacts to CdTe are a combination of the alternatives to ϕ_b choice, doping and surface charge modification.

In the second method pseudo-ohmic contacts are formed by doping the CdTe adjacent to the contact highly p-type to promote tunneling. This is usually done by modifying the CdTe surface to be Cd deficient, whereby dopants can be incorporated to occupy the vacant Cd sites.

4.3 Specific Contacts to CdTe

In this section a detailed review of literature and discussion of some of the typical materials used as back contacts to CdS/CdTe solar cells is presented.

4.3.1 Gold Contact

One of the most researched contacts is gold. It is either used alone or as a final metal layer applied after various surface treatments. They are formed using two methods:

1) Chemplating in a gold ion solution.
2) Vapor deposition of gold or Au-Cu alloy on a previously prepared surface of CdTe.

In the first method, it has been found that the cadmium diffuses out of CdTe with the simultaneous diffusion of gold into these vacancies providing the required extrinsic p-type doping. Another possibility is the formation of a thin layer of $AuTe_x$ that either forms the actual contact or helps to lower the barrier height. In the second method the cadmium vacancies are created using an etchant like $HNO_3/HCl/H_2O$, followed by the vapor deposition of Au or Au-Cu alloy to form the contact. The etching procedure is found to leave a tellurium rich surface that significantly reduces the resistivity of the thin layer adjacent to the contact. The use of the Bromine/Methanol etch was found to increase the R_c values, although yielding higher V_{oc}'s.

Copper and Au can also be sequentially deposited by PVD techniques followed by annealing, to form the contact. H.C.Chou et al [19] describes the nature of copper in these contacts. In his study of the effect of Cu thickness on cell performance, he observed that both series (R_s) and shunt (R_{sh}) resistances reduced with increase in Cu thickness. The improvement in the R_s was attributed to the formation of a better contact due to the increase in carrier concentration both at the contact interface and in the bulk. However the reduction of R_{sh} was assigned to the migration of excess copper to the CdTe/CdS

junction, where it forms shunting paths, and recombination centers. This causes the deterioration of junction properties and hence the cell performance. Secondary ion mass spectroscopy(SIMS) of cells with varying copper thickness corroborates this theory. From the SIMS results it was found that copper penetration into CdTe had a diffusion-like profile[20]. The diffusion process was aided by the polycrystallinity of the material, and the fact that Cu has an atomic size close to Cd. This suggested Cu diffusion could be along grain boundaries. The diffusion process was further enhanced by the out-diffusion of Cd during the metallization process. Further evidence on this grain boundary enhanced diffusion was obtained, when CdTe of different crystallinity (different grain sizes) exhibited different diffusion profiles. SIMS results comparing the Cu profiles in CdTe of different crystallinity is shown in figure 20.

Thus the conclusion derived from the work was that, the copper seemed to play a dual role in these contacts. On the one hand, copper plays a very important role by acting as a substitutional acceptor for cadmium thereby increasing the doping concentration near the surface of p-type CdTe. On the other hand it proves detrimental to device performance by forming interstitials or defect complexes, which act as recombination centers.

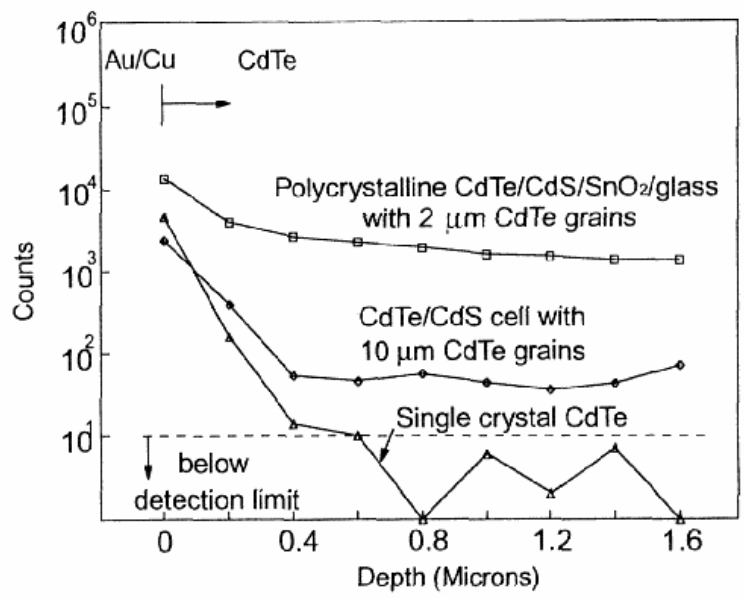


Figure 20 Cu SIMS Profile in the CdTe Layers with Different Degrees of Crystallinity

In a further study of these contacts, an interesting observation was the lack of dependence of Cu diffusion with the annealing temperature, although annealing was found to be useful in providing energy for Cu interstitials to occupy substitutional sites [20]. This facilitated an increase of the carrier concentration of CdTe. In addition, it was felt that the annealing process aided the formation of p^{+}-Cu_xTe, which reduced contact resistance.

The diffusion of Cu in single-crystalline (SC) and poly-crystalline (PC) CdTe is characterized by different mechanisms. Cu is considered to be a fast diffuser in SX CdTe (Diffusion Constant ~ $3 \times 10\text{-}12$ cm^2/s). In CdTe, Cu is reported to exist as an interstitial ion, Cu_i^{+}, giving rise to a shallow donor state or to substitute for a Cd atom to form a deep acceptor state. It is also thought to form complexes of Cu_i^{+} - Cu_{Cd} and Cu_i^{+} - V_{cd}^{2-}. In

addition, fast and slow diffusing components due to the Cu_i^+ and complex formation respectively have been identified. Other researchers argue that the high diffusion coefficients are due to Te precipitates or more generally due to extended defects present in defective crystals. In PC CdTe, the diffusion of Cu is expected to be higher due to the presence of grain boundaries. The grain boundaries allow for easier diffusion than the bulk due to weaker bonds formed as a result of incomplete coordination. Another factor affecting the diffusion of Cu is the presence of an electric field as one finds in p-n junctions. Thus polycrystalline CdS/ CdTe solar cells using copper contacts are affected in this regard. Despite the extensive research and the low R_c's obtained using the copper/gold contact, its effectiveness is not predictable and is very unstable. This has led to the search of other reliable contacting materials.

4.3.2 Li-Diffused Gold Contact

Lithium, a group I (alkali) metal acts as a p-type dopant in CdTe, and is thus a potential contact material. It has been deposited either using MOCVD (n-butyl lithium) or by vacuum deposition by evaporating lithium chromate or nitrate. The work of Bube et al, on the performance of lithium contact in SC CdTe, indicates that the contact resistivities of $0.01\Omega\ cm^2$ can be obtained using this contact [21].

It was found that the final resistivities were quite independent of the starting CdTe resistivity, suggesting that a highly p-type layer is formed at the contact interface. The contact was found to be ohmic at room temperature but deteriorated at lower temperatures (about 80K) due to the probable freezing out of holes and hence the tunneling current.

Although the Li contact was quite effective on fabrication its time stability left a lot to be desired. This effect is shown in figure 21, where the contact and sheet resistivities are plotted against time.

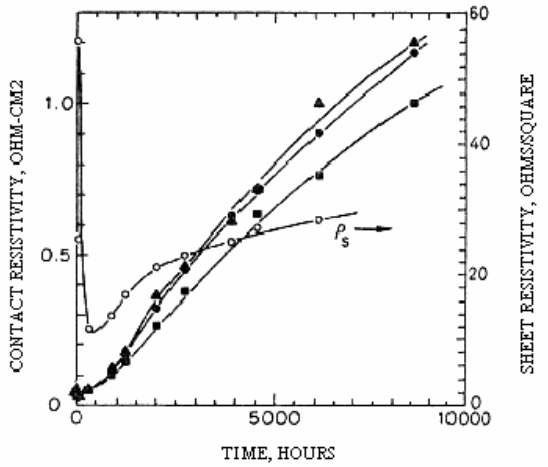


Figure 21 Contact and Sheet Resistivity for Li Diffused Contact on CdTe

o- sheet resistivity ● & ■ - $K_2Cr_2O_7$ Δ- Bromine in methanol

This deterioration was attributed to the loss of substitutional Li impurities through interaction with lattice defects or precipitation, compounded by the diffusion of the same from the contact interface.

4.3.3 ZnTe:Cu Contact

As suggested earlier, an interlayer of another suitable semiconductor could help provide a good ohmic contact. For this application, the interposed semiconductor must provide both a negligibly small valence band discontinuity with the p-CdTe, and also be easily doped heavily p-type at the outer metal contact, to promote tunneling.

Zinc Telluride, a p-type semiconductor with a direct band gap of 2.2eV has been used for this purpose. The formation of ohmic contacts to ZnTe is easier due to its lower work function and the ability to dope it highly p-type. Another attractive quality of ZnTe is the very low valence band discontinuity of –0.14eV with CdTe[22]. Thus it provides no hindrance to the flow of holes towards the contact. Zinc telluride films have been fabricated by a variety of techniques like MBE, MOCVD, electrodeposition, and RF sputtering. ZnTe is more easily doped by group V elements like P, As, and Sb than CdTe. However, copper is used to dope ZnTe for contact applications due to the added advantage of doping the CdTe bulk as compared to the group V materials. Carrier concentrations of 10^{19}-10^{20} cm^{-3} have been obtained in ZnTe:Cu films[23]. Figure 22 shows the energy band diagram elucidating the main components and function of p-ZnTe : Cu interface layer.

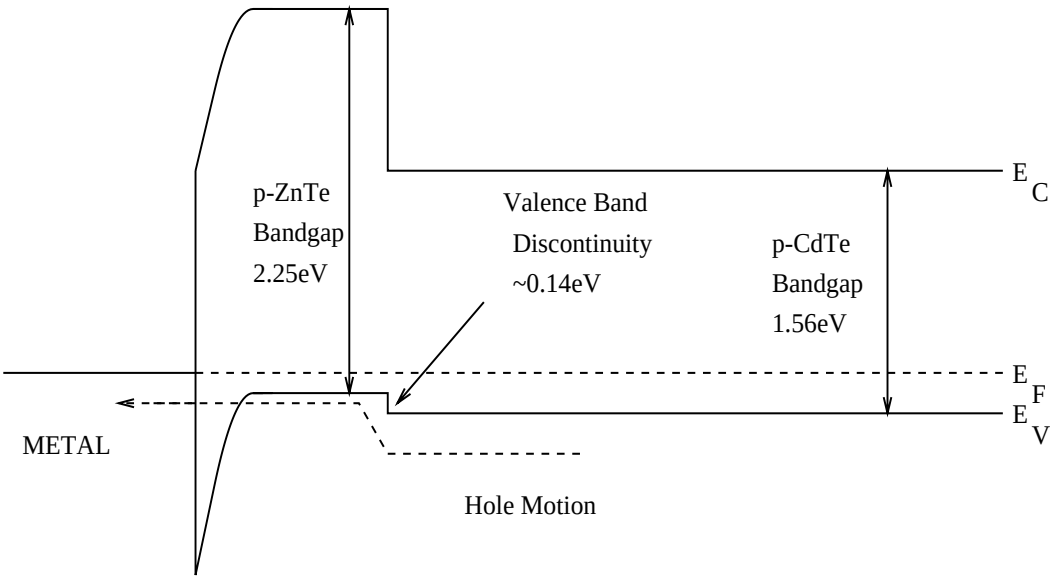


Figure 22 Band Diagram of CdTe/ZnTe Interlayer

A number of research group have fabricated solar cells with ZnTe:Cu contacts, exhibiting conversion efficiencies greater than 10%. T.A.Gessert et al, at the National Renewable Energy laboratory (NREL) obtained cells with efficiencies of 12.1%[24]. The Cu doped ZnTe films were fabricated by RF sputtering from a compound target of ZnTe and Cu where the Cu concentration was controlled. Studies on the electrical and compositional properties of the sputtered films indicated that a composition of Te/(Cu + Zn) = 1 provided films with lowest resistivities. At higher or lower values excess Cu or Te reduced the electrical quality of the film. For use in CdS/CdTe solar cell contact fabrication, a Cu concentration of 6 atm% provided the best results. It is believed that an alloy formation of $Cu_xZn_{1-x}Te$ where x = 0.6 possesses improved intra-grain quality compared to the films that contain excess Cu or Te. It was also observed that although the films had the highest electrical quality the efficiency of Cu incorporation was less than 50%. This meant that bulk of the Cu was electrical inactive. Thus the possibility of Cu diffusion toward the CdS/CdTe junction with time becomes imminent.

J.Tang et al proposed a vacuum evaporation method of forming ZnTe/ Cu/ metal contacts with conversion efficiencies as high as 12.9%[25]. The effect of ZnTe and Cu thickness, the post deposition anneal and the effect of the final metal contact were studied. It was observed that a copper concentration of 4.3 – 7.5% provided similar results above which the FF reduced. Post deposition anneals of 200ºC and below was found to be necessary to obtain high efficiency cells. Ni and Au, the final metals used for fabricating cells, interestingly very different results with the Ni contacted cells always providing lower Voc and FF.

Studies performed on the ZnTe contacts indicate that the stability of these cells vary with the kind of final metal layer deposited on them in addition to being critically dependent on the free copper content in the ZnTe[25]. Cells with Cu in excess of 6atm% in ZnTe showed greater degradation due to the migration of copper to the junction. Further, cells with Au metal layer were found to be more stable from an efficiency standpoint, although the cells with Ni showed slower R_s and doping level degradation. This was attributed to the inter-diffusion at the ZnTe/Metal layer in the case of Au cells, which seemed to act as a "getter" for copper. Thus less copper was free to diffuse towards the junction. Thus the stability studies indicate that the effectiveness of the ZnTe contact is questionable due the similar problems of the Cu/Au contact, although less severe.

4.3.4 HgTe Contact

Mercury Telluride, a semi-metal, with a reported work function of 5.9eV is ideally suited for forming ohmic contacts to CdTe[26]. In addition it has a nearly matched lattice parameter with CdTe (-0.3% mismatch)[27], with which it forms solid solutions over the whole composition range. HgTe, being a semi-metal, graded heterojunctions could be expected to behave as ohmic contacts. This holds for the HgTe-metal interface too.

HgTe has been used successfully as low-resistance contact to p-type single crystalline CdTe of 10-15 Ω-cm resistivity by Janik et al, using the close spaced isothermal technique. The contacts obtained using this technique possessed room temperature R_c of 0.1 Ω-cm^2 [27]. The equilibrium energy band diagram of the resulting CdTe/HgTe/Au structure is shown in figure 23. Although there exists a valence band

discontinuity of about 0.35eV for abrupt CdTe/HgTe junctions, as shown in the band structure there exists an inter-diffusion zone, which helps suppress the potential barrier providing a non-rectifying contact.

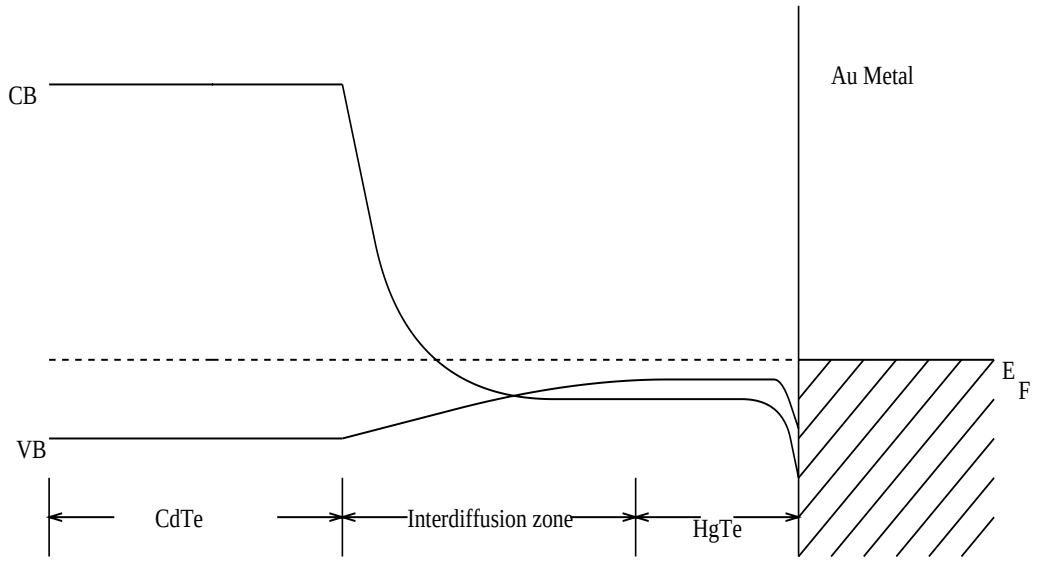


Figure 23 Equilibrium Energy Band Diagram of CdTe/HgTe/Au Interface

Despite the low Rc's obtained using this technique, it could not be used for polycrystalline CdTe solar cells due to the high processing temperatures involved in forming the HgTe layer. The temperature of 550ºC used for the deposition actually caused structural changes in the CdTe crystals.

Chu et al successfully used the CSS and CVD techniques for depositing HgTe on PC CdTe using relatively lower processing temperatures (300ºC)[28]. CdS/CdTe solar cells fabricated using the CSS technique for contact fabrication yielded conversion efficiencies of 10.6%, with the contact resistivity of 0.4-0.8Ω cm^2. As promising as it was, the CSS process was extremely slow and often led to shunting of devices due to the

long time for deposition. Further, the thermal instability of HgTe made the process more complicated. Although stability studies on these contacts were not done, the lack of repeatability of performance was a major deterrent to this technology.

4.3.5 Doped Graphite Paste

World record efficiencies have been obtained using graphite paste doped with a mixture of HgTe:Cu. It is believed that interlayers of Cu_2Te and $Hg_{1-x}Cd_xTe$, that are highly p-doped, help tunneling of holes across the contact [29]. J Britt and Ferekides et al, at the University of S. Florida, developed an effective procedure for fabricating these contacts, consisting of a brief etch of CdTe before the application of the contact paste [30]. The cells were air dried after the contact application, following which, the samples were annealed at 275ºC in He atmosphere for 25 min. The variation of the cell parameters with the type of semiconductor mixed in the graphite is summarized in table 4

Table 4 Cell Performance vs Contact Material

Semiconductor	Open Circuit Voltage, mV	Short Circuit Current, mA/cm2	Fillfactor, %	Efficiency, %
HgTe	836	20.16	74.59	12.6
HgTe &CuTe	840	21.8	70.6	12.9
HgCuTe	842	24.13	74.17	15.1
HgTe:Cu	858	23.62	74.61	15.1

It can be seen that fill factors above 70% could be routinely obtained using the above procedure. The variation of current densities was attributed to the variation in the CdS thickness and not related to the contact. The performance of the contact was found to be critically dependent on the CdTe etching procedure and the annealing temperature and time. The etching procedure helps provide a tellurium rich surface to enable contact formation, although the time and concentration of the etch need to be controlled, to prevent excessive etching along the grain boundaries. The contact anneal dictated the extent of reaction at the CdTe surface in addition to affecting the diffusion of the contact material into the CdTe. The highest fill factors obtained using the above procedure was 76% and the best conversion efficiency was 15.8%. The contact, however, is bulky and hence more difficult for use in modules. In addition, it is unstable over long periods of time due to the presence of Cu.

4.3.6 Diffused Copper Contact

As is evident from the discussion of some of the contact procedures, copper is used in conjunction with other materials to aid contact formation. However, copper can be used as is, for contact fabrication. The diffused copper contact proposed by McCandless et al [31], consisted of deposition of elemental Cu layer on the CdTe surface, heat treatment of entire structure, etching in Br/Methanol solution to remove elemental copper, and application of a desired current –carrying contact material like Ni, Cr, Pt, Mo, or ITO.

No systematic dependence of device parameters or efficiency with the contact material was found, indicating no influence of contact material function. This, together with the low resistance measured, indicated that a very conductive surface was obtained after etching and was thus insensitive to the type of the final metal deposited. Thus novel designs, such as transparent cells, could be fabricated using this approach. Fill factors up to 77% was obtained using the diffused copper contact process.

Stability studies of this contact need to be performed before an evaluation could be made on them, however, since the etching procedure is reported to remove any elemental Cu it suggests that these devices could resist degradation to a greater extent.

4.3.7 The Cu_2Te Contact

Contacts that use elemental Cu are characterized by the formation of a p+-Cu_xTe layer at the interface between CdTe and the metal. Previous work undertaken at USF was aimed at forming this layer on CdTe by the process of sputtering from a compound target of Cu_2Te as opposed to its formation by post deposition heat treatment. The objective of this method was to limit the amount of free Cu, and as a consequence, reduce the degradation of the junction with time. The EDS analysis of Cu_2Te films on glass suggested that stoichiometric compositions were obtained at a deposition temperature of 250ºC. Higher temperatures lead to copper rich stoichiometries. The contact characteristics, and hence the device results, were influenced by temperature of Cu_2Te deposition, thickness, and the post deposition annealing. The effect of Cu_2Te deposition on device performance is shown in table 5 [32].

Table 5 Effect of Cu_2Te Deposition Temperature on Cell Performance

Substrate Temperature, (ºC)	Voc, (mV)	FF, (%)
200	791	65.3
250	825	69.3
300	700	54.7
350	346	34

The results suggest the existence of an optimum temperature of 250ºC for best device performance, which corresponds to the temperature at which the correct stoichiometry was observed. Higher temperature lead to shunted devices, probably due to the excess copper diffusion towards the junction. The post deposition anneal was important in that it provided any free Cu, that might be present, the energy to dope the CdTe.

The major advantage of the Cu_xTe/Molybdenum contact was the ease of fabrication, and its ability for large-scale manufacture [33]. In addition, it was an improvement over the graphite paste contacts used earlier because it provided a better coverage of CdTe. This is illustrated in Figure 24.

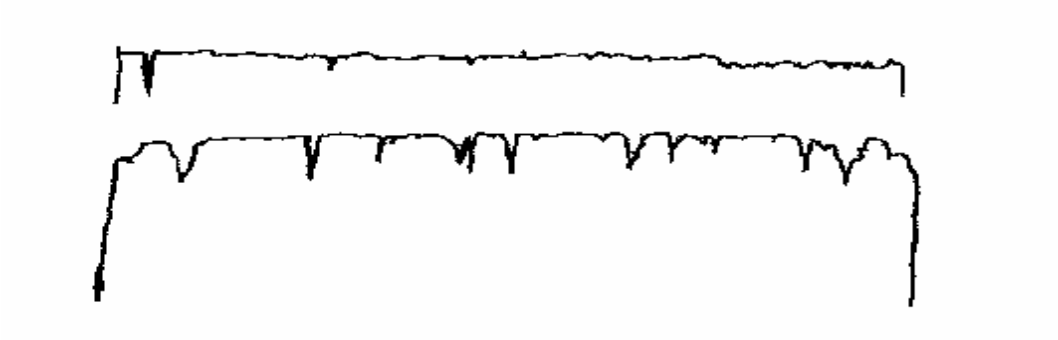


Figure 24 OBIC Scans of CdTe Cells with Cu_xTe/Mo (top) and Graphite (bottom) Contacts

This in turn could improve the J_{SC} obtainable from the cell. Although stability studies on these contacts are presently underway and the results very preliminary, there is some evidence of rectification of these contacts with time, which may be linked to the movement of Cu from the contact interface to the bulk.

4.4 Copper Contacts – A Summary

From the above discussion of some of the contemporary contacts, it is evident that Cu is successfully used either in elemental form or in conjunction with other materials. High efficiencies have been obtained using Cu by a number of research groups, but the cells degrade with time and are hence unreliable. This is due to the diffusion of copper toward the junction causing degradation. For CdS/CdTe solar cells to be commercially viable it is thus important to address the reliability issue related to copper. However it is more lucrative to find other alternative contacting materials and procedures that could result in a stable and low resistive contact to CdTe.

4.5 Copper-Free Contact Alternatives

The first step towards more reliable contacts is to get away from the use of copper in contact fabrication. The development of a Cu-free contact technology should thus either involve the incorporation of other materials in CdTe to dope it p-type, or the use of other semiconductor materials that could provide the proper interface between the CdTe and the metal. Group-I elements (transition) can provide p-type doping by replacing Cd in the lattice, whereas Group-V elements can perform the same by replacing Te in the lattice. Although straightforward in concept, as discussed earlier, the incorporation of these elements in poly crystalline CdTe is difficult.

Some of the elements of interest that have been incorporated in single crystalline CdTe during growth include Antimony (Sb), Arsenic (As), Nitrogen (N), or Phosphorous (P). Unfortunately, the translation of these processes to poly crystalline CdTe have not yet been successfully achieved. Some of the contacting technologies that use materials other than Cu are presented below.

4.5.1 Ni-P Contacts

The electrodeless deposition, a technique widely used for deposition of Ni on metal, surface was adopted by B.Ghosh et al for contact fabrication to CdTe. It involved the autocatalytic reduction of Ni in the presence of a hypophosphite. In his study the author observed that the growth of Ni-P layers on CdTe was dependent on the solution constituents, pH, and the temperature of the solution [34].

Microstructural analysis of the contacting interface using XRD revealed the presence of several peaks corresponding to NiP, $NiTe_2$, NiP_2, and P. The effect of annealing on the interface is shown in figure 25.

Optimum contact properties were obtained at 250ºC.The improvement of the contact properties at annealing temperatures of 250ºC was attributed to the formation of a favorable phase NiP_2 at these temperatures. It is clearly seen from the figure that the peak corresponding to NiP_2 becomes more prominent at 250ºC. This phase is believed to posses a work function as high as Au thereby improving contact properties. In addition at these temperatures the diffusion of phosphorous in the vicinity of the contact helps to dope the CdTe region more p-type. This facilitates the formation of a tunneling contact. Annealing temperatures in excess of 250ºC however increased the contact resistance probably due to the precipitation of Ni_3P layer. The effect of phosphorus on these contacts is still a speculation and needs careful analysis. Although the Ni-P contacts hold promise solar cells fabricated using the Ni-P contacts have yielded V_{oc}'s of 600mV and fill factors of 50% only[35].

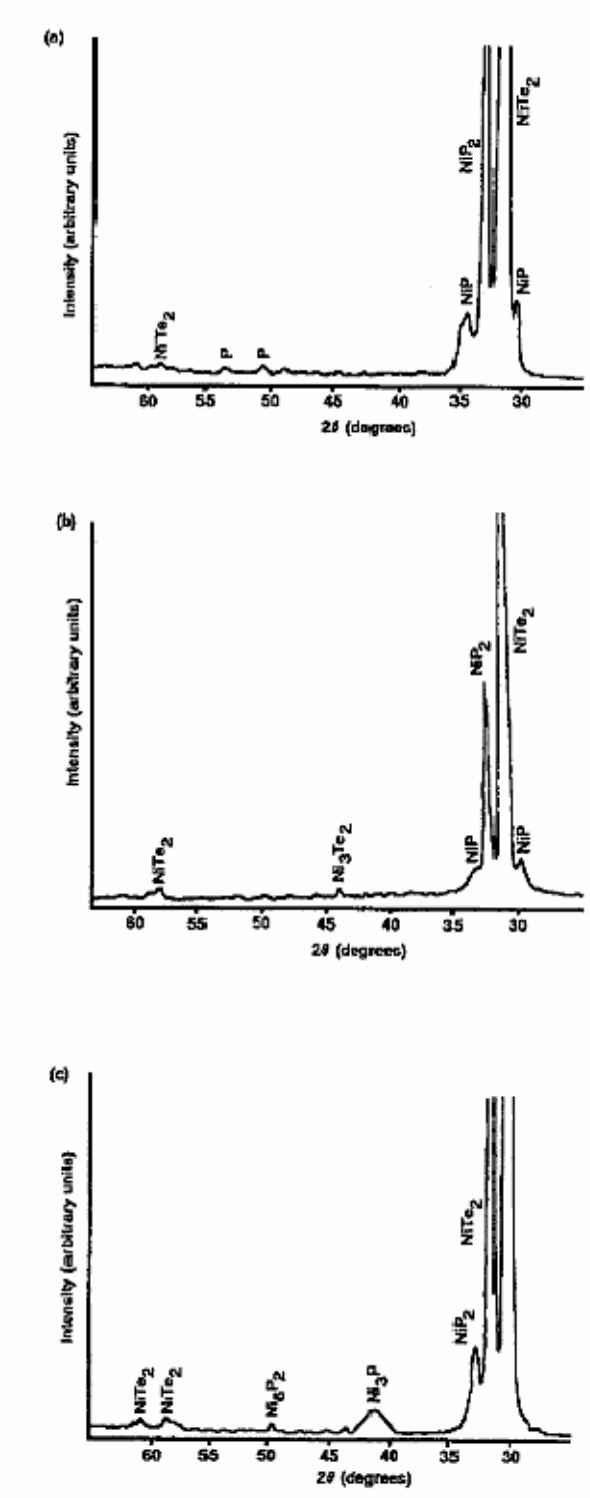


Figure 4. X-ray profiles of a Ni–P/CdTe contact (*a*) just after deposition, (*b*) after annealing at 250 °C for 90 min and (*c*) after annealing at 350 °C for 50 min.

Figure 25 Effect of Annealing on Ni-P/CdTe Contact Interface

4.5.2 Sb_2Te_3 Contacts

Sb_2Te_3, a p-type semiconductor with a low optical band gap of 0.2-0.3eV has been used for contacts for CdTe solar cells. Study of Sb_2Te_3 films on amorphous substrates like glass was done by Mandouh et al [36]. He found that the as deposited films were amorphous, but annealing of these films at 200ºC had a profound effect on their crystallinity. He also observed a reduction in the resistivity of the Sb_2Te_3 films with thickness. This was attributed to the formation of a more homogenous layer at greater thickness. Work done by Roy et al on single crystals of Sb_2Te_3 showed that carrier density obtained in this material is of the order of 10^{20} cm^{-3}[37].

The mechanism of contact formation using Sb_2Te_3 is not understood due to the lack of sufficient knowledge of the material properties. However, Sb_2Te_3 contacts have been successfully fabricated at the physics department of the University of Parma, Italy. Romeo et al deposited Sb_2Te_3 films on CdTe solar cells at substrate temperatures of 300ºC, by RF sputtering of a compound target of Sb_2Te_3 [38]. The resistivity of these films was 10^{-4} Ω cm at these conditions indicating that the material was highly p-type. The final metal layer was Molybdenum, also deposited by RF sputtering. Cells fabricated using this method yielded Voc = 857mV, FF = 73%, Jsc = 24.5mA and efficiency = 15.1% on soda lime glass substrates. Stability studies on these cells we performed by soaking them at 1sun for six months resulted in no change of the photovoltaic properties indicating the long-term reliability of these contacts.

Work done by T.Schmidt et al on the chemical stability of Sb_2Te_3/ Ni contacts using phase diagram calculated from Gibbs free energy criteria, showed that the CdTe/

Sb_2Te_3 interface was in thermodynamic equilibrium. Thus it is not easily degenerated by chemical reactions. However, the Ni/Sb_2Te_3 interface was found to be in non-equlibrium leading to spontaneous formation of $NiTe_X$, $NiSb_X$ and Sb_2O_3. This seems to suggest that the long-term reliability could be in question as the non-equilibrium could cause reaction products that increase the contact resistivity thereby reducing the cell efficiency [39]. Similar studies on the Sb_2Te_3/Moly contact could help determine the chemical stability of the contact.

4.6 Contact Etching

The etching of CdTe surface is a critical step in the process of contact fabrication. It is usually performed prior to contact fabrication and thus determines the effectiveness of the contact to a certain extent. In this section a brief overview of the basic physics and chemistry of etching is provided followed by a detailed literature review of the etching procedures typically used for CdTe over the years.

4.6.1 The Etching Process

Etching, in microelectronic applications, is a process by which material is removed from a given substrate by chemical reaction with a reagent material called an etchant. Etching processes can be classified into *wet* and *dry* etching based on the medium used, and into *isotropic* and *anisotropic* based on the direction of etching.

Wet chemical etching was the standard technique used for early integrated circuits due to the knowledge gained on it by the printing industry. In addition, it provided good

selectivity between materials. However, the isotropic natures of these etches limited their use in certain applications. This led to the advent of dry etching which offered the capability of anisotropic or directional etching. Over the years dry etching has gained overwhelming importance due to the additional manufacturing advantages of eliminating handling, consumption and disposal of large quantities of acids and other solvents used in wet etching. Wet etching has been predominantly used to etch CdTe for solar cell applications; however dry etching is gaining increased attention mainly due to the better integration in the assembly during manufacturing. There are many types of dry etching based on the mechanism of the etching process, like

1) Physical sputtering and Ion beam milling
2) RIE(reactive ion etching)
3) Plasma Etching.

Physical sputtering provides a very anisotropic etch due to the strong directional nature of the energetic ions, although the selectivity is quite poor. In addition, it also suffers from the accidental re-deposition of non-volatile species on the substrate. In RIE, the etching mechanism is strictly chemical and thus provides very good selectivity, although they are isotropic. By adding a physical component to a purely chemical mechanism the shortcoming of both the above dry processes can be eliminated. This is the basic idea of the plasma etching process, which is described in greater detail in the next sub section.

4.6.2 Basic Physics and Chemistry of Plasma Etching

The basic concept of the plasma etching process involves an RF flow discharge that produces chemically reactive species (atoms, radicals and ions) from an inert molecular gas. The etching gas is selected to generate species that chemically react with the material to be etched, and whose reaction product is volatile. In cases where the reaction product is non-volatile a physical component is added to principally enhance the etching process by ionic bombardment. Thus the process is an ion-assisted etching process. It is thus important to note that the radicals produced by the plasma, and not by the ion bombardment basically provide the etching.

In plasma systems high frequency (e.g., 13.5 MHz) rf-diode configurations are primarily used. The knowledge of the potential distribution is useful because the energy with which the particles impinge on the etched surface depends on it. It also determines the energy with which ions strike other surface in the chamber, which could in some cases cause re-deposition of sputtered material as contamination. The potential of the plasma is positive relative to the grounded electrode, while the powered electrode develops a negative self-bias with respect to the ground. The magnitude of the self-bias depends on the magnitude of the RF signal. If the electrodes of the RF plasma systems are of comparable area, the potential difference across the dark space of both the electrodes will be equal. Since the powered electrode develops a negative dc self-bias voltage, in order for a potential difference of equal magnitude to exist across the dark space of the grounded electrode, the plasma must assume a positive potential of comparable magnitude. Even if the substrate is placed on the grounded electrode of these systems,

they will still be subjected to substantial energetic ion bombardment. In systems where the area of the powered electrode is much smaller than that of the grounded electrode, smaller potential differences exist between the plasma and grounded electrode, and thus the grounded electrode undergoes less bombardment. The reactive as well as the ionic species are produced in such plasma. In dry etching processes heterogeneous reactions (reactions at the substrate surface) are more favored, and the interactions of the gas phase species and the substrate material cause etching. The basic tenants of this mechanism is

(1) The sticking coefficients of the radicals and ions on substrate surface

(2) Chemical recombination processes that form films, cause species to be adsorbed, or lead to other gas-phase species

(3) Process of adsorption, reaction at the surface and formation of volatile etch products

(4) Desorption from the substrate surface facilitated by the energetic ion bombardment

Other factors that influence the heterogeneous reactions include surface temperature, surface potential, nature of surface and the geometric aspects of the surface.

4.6.3 Etching of CdTe

Etching CdTe prior to contact application has found to be necessary to obtain better contact formation. The most widely and successfully used approach for CdTe etching has been wet chemical etching in a suitable solvent. A number of solvents have been used for this purpose like the Bromine in Methanol, $HNO_3/H_3PO_4/H_2O$, and

K2Cr2O7/H_2SO_4 solutions. The basic mechanism of these etching solutions is the selective removal of cadmium, leaving either a tellurium rich layer or a conductive tellurium film. This helps reduce the contact resistance of the resulting contact. In this section a brief review of research done in this regard is presented.

In order to illustrate the effect of the CdTe surface composition on the back contact properties Dean Levi et al at NREL fabricated devices under similar conditions, but for the final surface preparation prior to contact fabrication [40]. In particular he studied the effect of the type of $CdCl_2$ treatment (vapour chloride or solution $CdCl_2$) and the effect of nitric acid and N/P etch. The different sample surfaces were analyzed using X-Ray Photoelectron Spectroscopy (XPS) depth profiling, to determine the concentration of the various elemental species like Te, Cd, O_2, Cl, and C. The study revealed that the as-deposited samples had a Cd/Te ratio considerably greater than 1. The ratio reduced to stoichiometric proportions with depth profiling. The higher Cd/Te ratio meant that the surface was probably n-type providing an explanation for the reason for poor contacts obtained in the absence of a pre-contact etching procedure. The solution grown $CdCl_2$ treated CdTe (SCC) after annealing possessed the highest Cd/Te ratio in addition to the higher oxygen content indicating the substrate surface is probably oxidized considerably. The vapor $CdCl_2$ treated sample (VCC) had considerably less oxygen compared to the SCC. However, irrespective of the sample surface prior to the nitric or N/P etch the etching process results in similar surfaces that are tellurium rich. Device fabricated using the experimental surfaces were measured for performance and tabulated in table 6 follows.

It can observed from the above table that the samples etched in the N/P etch exhibit the lowest series resistance. This was attributed to the formation of a thin layer of Te formed on the CdTe surface as determined using the XPS study.

Table 6 Effect of Surface Preparation on Device Performance

Sample Processing	Rs(Ω-cm^2)	Efficiency(%)	FF(%)	Voc(mV)	J_{SC} (mA/cm^2)
As Deposited	7.0	8.7	55	719	22
SCC only	NA	NA	NA	NA	NA
SCC/Anneal	6.9	12.05	63.3	812	23.5
SCC/Anneal/DI	8.0	12.35	65.5	815	23.4
SCC/Anneal/Vacuum anneal	6.8	11.9	61.8	808	23.8
SCC/Anneal/DI/HNO_3	5.3	12.85	66.3	818	23.7
SCC/Anneal/DI/NP etch	1.3	13.05	69.7	804	23.2
VCC only	2.5	13.1	68	820	23.6
VCC/vacuum anneal	3.2	13.1	67.1	818	23.8
VCC/DI	3.7	12.25	63.5	818	23.5
VCC/DI/HNO_3	2.9	12.5	65.2	816	23.4
VCC/DI/NP etch	1.7	13.3	71.2	816	22.7

4.6.3.1 The N/P Etch

The effect of the N/P etch was also studied in greater detail by Sarlund et. al. in his work to establish the mechanism of the etching process[41]. He observed that there was a certain induction period before any discernable change in the CdTe resistivity. This was attributed to the removal of oxide that forms on the untreated CdTe surface. After this period, bubbles started to form on the surface when observed under an optical microscope. The bubbles grew bigger with the etch time, eventually becoming large

enough to be seen using naked eye. The origin of bubbles was attributed to the formation of gaseous bye-products. At this time the surface was found to change color from dark gray to a silvery gray tinge. Again, with further etching this color became more predominant. The films measured after the etching exhibited considerably lower resistivities. In order to determine the cause SIMS depth profiles were obtained. These indicated the formation of a tellurium rich layer whose thickness depended on the etch time. The XRD patterns of these films confirm the formation of hexagonal Te on the CdTe surface.

In order to determine the role of the constituent acids used in the process different compositions were studied. In cases where only one of the constituents were used no discernable changes were observed indicating that both the acids played an important role in the etching mechanism. Since the main component H_3PO_4 does not possess a strong oxidizing power as the HNO_3, the minor component, the role of HNO_3 as an oxidizing agent was quite evident. The H_3PO_4 merely acted as a proton source to provide acidic conditions to favor the reactions leading to the desired products. The role of HNO_3 as an oxidizing agent was verified by substituting it by another oxidizing agent like H_2O_2. Although the surface colour change was not clearly observed XRD analysis revealed formation of surface Te (also confirmed by the reduction in the resistivity). The replacement of H_3PO_4 was studied by replacing it by H_2SO_4, CH_3COOH, and HCl. It was observed that crystalline Te was formed with sheet resistances of 24kΩ/sq when CH_3COOH was used to replace H_3PO_4. The use of HCl to replace H_3PO_4 was unsuccessful due to uneven etching, formation of $CdTeO_3$ and partial flaking of the film.

When H_2SO_4 was substituted, the color change was quicker but was temporary. This was explained by the strong oxidizing property of H_2SO_4, which causes formation of $CdTeO_3$.

4.6.3.2 The Br/Methanol(BM) and Potassium Dichromate(KD) Etch

A systematic study of the effect of the BM (0.1% Br) and KD etch ($K_2Cr_2O_7$:H_2SO_4 :: 1:1) was done by Danaher et al on single crystal and thin film CdTe[42]. The study on the BM etch revealed that the thin film etched more rapidly than the single crystal probably due to enhanced etching along grain boundaries in the thin film. The XPS spectra showed a reduced Cd/Te ratio in both crystal and thin film indicating preferential removal of Te. Depth profiling indicated that the Cd depletion regions in the film were deeper than the single crystal resulting form the predominance of etching along the grain boundaries in the thin film. In addition, the XPS spectra also revealed the formation of etch residue ($CdBr_2$) on both the film and single crystal surface in case where the samples were not washed after etching. On washing in Br/Methanol for 4min the residue reduced significantly. More extensive cleaning was however not beneficial due to the formation of hydroxides on the surface, which prove detrimental to contact formation. Thus it was inferred that the etch time, washing procedures are critical to obtain the desired surface. The KD etch was found to be more aggressive than the BM etch with deeper Cd depleted regions observed. The KD etch left a Te rich surface, with TeO_2, and elemental Cr as the etch residue, the concentration of which could be significantly reduced by making the etchant sufficiently acidic. The etch time could be altered by varying the K_2Cr_2O7 concentration in the etchant.

4.6.4 Dry Etching of CdTe

Although, the use of wet chemical etching is widespread and quite effective, it is less preferred for large-scale manufacture. The development of a dry etching procedure for CdTe in solar cell manufacture could help overcome this limitation. Dry etching techniques are part of standard processing in IC manufacture. However, there are few dry etching techniques that have been used for single crystal CdTe. The incorporation of dry etching techniques could help development of an all-vacuum process for CdS/CdTe solar cells.

4.7 Motivation

From the detailed review of literature presented, it could be realized that the problem of contacting to CdTe is quite complex. The contact containing copper seems to provide the best option, but is not very reliable for use of the CdTe cells for long-term terrestrial applications. Thus the future of this technology will need to involve new contacting materials that can answer both performance and stability issues. Work done elsewhere on the use of semiconducting materials like Sb_2Te_3 and Ni-P has provided a new direction in the quest for a suitable contact to CdTe. As promising as the materials are, they need to be researched in greater detail before their suitability to CdTe can be confirmed. The motivation for this work is to perform a detailed analysis on the suitability of these materials as contacts for CdTe cells fabricated at University of South Florida. The work would thus involve the comprehensive study of the contact properties, effect on cell performance, and the long-term reliability of these contacts.

CHAPTER 5

CELL FABRICATION PROCEDURE

Figure 26 below shows the schematic of the superstrate configuration of a CdS/CdTe solar cell fabricated on 7059 glass.

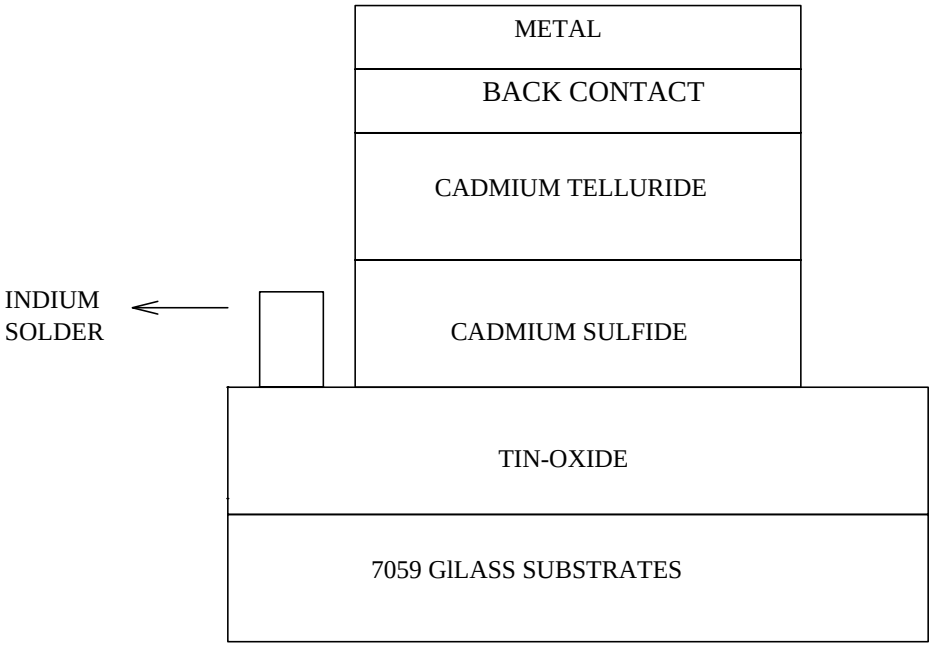


Figure 26 Schematic of CdS/CdTe Solar Cell (Superstrate Structure)

The cells used for this work were fabricated on high purity 7059 boro - silicate glass with a high transmission coefficient of about 95%. On the 7059 substrates a transparent conducting oxide (TCO), which conducts the current from the CdS/CdTe

junction to the front metal contact, is deposited. The TCO used is SnO_2, which is deposited by MOCVD. The source of Sn is a metalorganic precursor, tetra methyl tin (TMT), and the halocarbon 13B1 serves as the source of fluorine, which acts as the dopant. Helium and oxygen are the ambient gases for the deposition. The deposition of SnO_2 is a bi - layer process with the doped and undoped layer deposited sequentially. The final thickness of SnO_2 is about 0.8 - 1μm and the sheet resistivity is about 7 - 10Ω /cm^2. The window layer, CdS, is deposited using the chemical bath deposition technique. The reactants used for this deposition are as follows.

1) Cadmium acetate, which is the Cd ion source.

2) Thiourea - the sulfur ion source.

3) Ammonium acetate(NH_4Ac) and Ammonium hydroxide(NH_4OH) - which acts as the buffer.

A mixture consisting of measured amounts of CdAc, NH_4Ac and NH_4OH solution is prepared. The process involves immersion of the SnO_2:F coated substrates contained in a glass holder into a reaction beaker containing specific amount of water. This system is then heated to 90°C and a measured amount of reaction mixture along with a known amount of thiourea is added at periodic intervals of 10 - 15 min. The temperature is maintained at 90°C at all time during the process. The rate of formation of CdS can be adjusted by varying the concentration of ammonia and NH_4 salt in the solution. It is desirable to have a heterogeneous formation of CdS, which provides very adherent films on the substrate as compared to homogeneous formation where the CdS precipitates in the solution forming powdery, and hence non-adherent films.

CdTe, the heterojunction partner, used in these cells was deposited using the close - spaced sublimation technique. This technique is based on the reversible dissociation of CdTe at high temperature

$2\ CdTe \Leftrightarrow 2\ Cd\ (g) + Te_2\ (g)$

Before the actual deposition, the CdS substrates are annealed in H_2 for about 10 min at 400°C. The CdTe source and the substrate are separated by a small distance with the source maintained at a higher temperature than the substrate. The CdTe at the source dissociates into its elements and recombines at the substrate, and the rate of transport is diffusion limited. The important parameters of the CSS techniques are

(1) Temperature of source and substrates.

(2) Pressure in the reaction tube.

(3) Separation of source and substrate.

(4) Composition of source material.

$CdCl_2$ is essential to improve cell performance. The effect of this treatment is to increase the CdTe grain size, which reduces the grain boundaries, shunting path and recombination and thus causes the betterment of device characteristics. It is also believed to improve the CdS/CdTe interface, thereby enhancing the V_{oc}. $CdCl_2$ deposition is done by the vacuum evaporation of $CdCl_2$. The deposition of $CdCl_2$ is followed a post deposition anneal at 400°C in He and O_2, for 45 mins.

5.1 Back Contact Formation

Before the fabrication of back contact the CdTe surface is modified. This involves the removal of excess $CdCl_2$ by rinsing in methanol. The CdTe surface is then etched using Bromine dissolved in methanol for about 10secs. This provides a tellurium rich surface that is necessary for the making a good low-resistance contact. The contacts experiment in this work were

1) ZnTe/Cu_2Te contacts
2) Sb_2Te_3 contacts
3) Ni_2P contacts

5.1.1 The ZnTe/Cu_2Te Contact

After the Br-methanol etch, the samples were loaded into a vacuum chamber for the deposition of ZnTe by RF sputtering. The substrate temperature during deposition was 300ºC, and the ZnTe thickness was about 1000-1500Å. This was followed by the deposition of Cu_2Te at substrate temperatures of 250ºC. Very low sputtering power was used in order to obtain better control of the Cu_2Te thickness. After the deposition of Cu_2Te cell areas were defined, followed by the deposition of molybdenum at room temperature for a thickness of about 8000Å. The cells were then subjected to a post deposition heat treatment at 200ºC for 15mins. The effect of Cu_2Te thickness and substrate temperature was studied.

5.1.2 Sb_2Te_3/Moly Contact

Before using Sb_2Te_3 for contact fabrication, depositions were carried out on glass in order to determine the effect of substrate temperature on the stoichiometry of the films. The deposition of Sb_2Te_3, on CdTe solar cells, was performed using RF sputtering of a compound target of Sb_2Te_3.The deposition thickness and temperature were varied to study their effect on device performance. The final metal layer deposited was molybdenum, typically 8000Å thick. The effect of post deposition anneal of these contacts was also studied in the temperature range of 200-400ºC.

5.1.3 Ni_2P Contact

High purity Ni_2P powder mixed in graphite paste was used as the contact material. This paste was painted over the etched CdTe surface and dried for a few hours to rid the graphite of its solvent. The cells were then annealed at temperatures ranging between 75-300ºC, to observe the influence on performance as a function of temperature.

After the fabrication of the contacts the cells were scribed to expose the SnO_2. Indium solder was then applied on this layer to form the front metal contact. Finally, the completed cells were characterized by I-V, C-V, and spectral response measurements. In addition secondary ion mass spectroscopy (SIMS) was performed on certain cells to obtain depth profile measurements.

CHAPTER 6

RESULTS AND DISCUSSION

Earlier work done at the University of South Florida involved the use of Cu_2Te/Moly as back contact for CdTe solar cells. The details of this work were briefly discussed in chapter 3. This chapter is organized as a continuation of the earlier work done at the Thin Film Solar Cell Laboratory at USF.

Initial stability studies on Cu_2Te contacts revealed the degradation of contact properties with time. As a further study of Cu_2Te for back contacts a modified ZnTe/Cu_2Te contact is presented in the first section followed by stability studies on these contacts. This is followed by the work done on Sb_2Te_3 and Ni_2P as alternate Cu-free options for CdTe solar cells. In the final section, a new dry etching process for CdTe back contact fabrication is discussed.

6.1 ZnTe/ Cu_2Te Contact (ZnTe Contact)

The stability problems associated with Cu_2Te contact were observed to be similar to the degradation processes occurring in Cu contacts, namely, by the diffusion of copper with time towards the metallurgical junction. In the case of the Cu_2Te contact, the excess Cu arising from the deposition process or the decomposition of the Cu_2Te layer over time, causes instability. To address this issue, the back contact with a modified structure was fabricated. After the CdTe etch, ZnTe was deposited prior to Cu_2Te deposition. As

discussed in the previous chapter, ZnTe doped with Cu has been successfully used for back contact fabrication. In this approach, the basic idea was to use the excess Cu, from Cu_2Te, for doping the ZnTe. To study the effect of the ZnTe contact, experiments were limited to the study of the influence of Cu_2Te thickness and deposition temperature on the cell performance. For this purpose, the ZnTe deposition conditions and thickness were kept constant (approximately 1500Å).

6.1.1 Effect of Cu_2Te Thickness

Table 7 gives the variation of V_{oc} and FF as a function of the Cu_2Te thickness.

Table 7 Effect of Cu_2Te Thickness on Cell Performance

Sample #	Cu_2Te thickness (Å)	Voc, (mV)	FF, (%)
3-12b-4	75	778	56.6
5-20a-2	100	837	65.2
5-20a-3	150	846	71.5

From table 7 it is evident that the V_{oc} and FF increase with the increase in Cu_2Te thickness. This is due to the improved contact obtained as a result of the decrease in the series resistance (at V_{oc}), as the thickness of the Cu_2Te layer increases. I-V curves of these cells shown in figure 27 indicate this behavior.

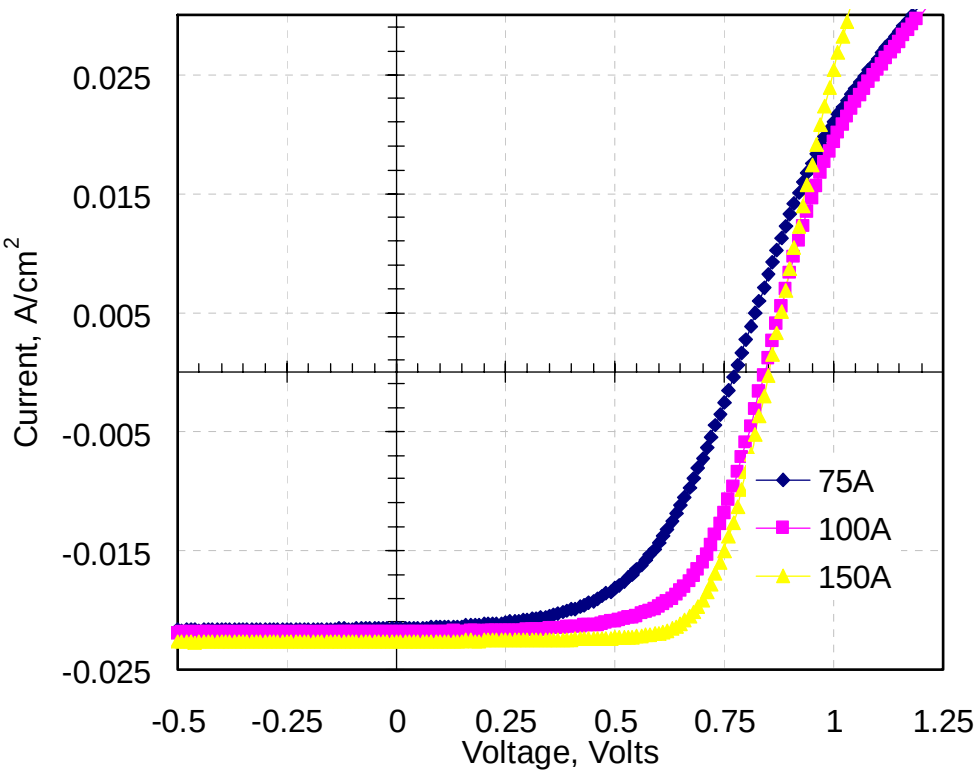


Figure 27 Effect of Cu_2Te Thickness on J-V Characteristics

Although is the presence of a back barrier is evident in all cases, it appears to progressively decrease as the copper thickness increases. Further optimization of the thickness could lead to complete elimination of the back barrier or reduce it to a point where it no longer affects cell performance. The reduction in series resistance is probably due to increased doping of ZnTe, as the Cu_2Te thickness is increased. This helps the formation of a tunneling contact as explained in chapter 2.

6.1.2 Effect of Cu_2Te Deposition Temperature

To study the effect of Cu_2Te deposition temperature on the characteristics of the ZnTe/Cu_2Te contact, Cu_2Te was deposited at two different temperatures, namely 250 and 350ºC. These temperatures were chosen to study the effect of the Cu_2Te composition on device performance. Based on earlier work done on Cu_2Te films, the Cu_2Te film deposited at 250ºC was found to be close to stoichiometry while that deposited at 350ºC was copper rich. Figure 28 shows the effect of this parameter on the I-V characteristics of the solar cell.

From the I-V characteristics it is evident that the cell with Cu_2Te deposited at 350ºC exhibits poor overall photovoltaic performance as compared to the cell at 250ºC. A closer look at the IV characteristics indicates that at reverse bias beyond -0.4V both curve start to show similar R_{sh}. However, in the 4rth quadrant, behavior of curve 1 clearly shows that the performance is collection limited (in addition to a higher series resistance).

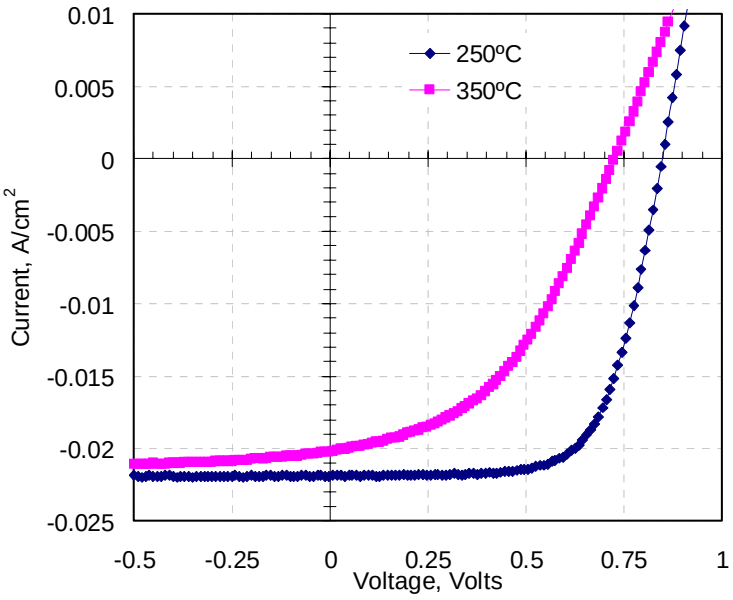


Figure 28 Effect of Cu_2Te Deposition Temperature on J-V Characteristics

In order to further understand this behavior, C-V measurements were performed on these cells to estimate the carrier concentration in the CdTe. The carrier concentration in CdTe as a function of both thickness and deposition temperature of Cu_2Te is tabulated in table 8.

Table 8 Carrier Concentration (in cm^{-3}) as a Function of Cu_2Te Thickness and Deposition Temperature

Cu_2Te thickness(Å)	Cu_2Te temperature	
	250ºC	350ºC
100	1.38×10^{14} cm^{-3}	6.9×10^{14} cm^{-3}
150	2.3×10^{14} cm^{-3}	6.9×10^{14} cm^{-3}

As is evident from table II the doping concentration increases with increasing Cu_2Te deposition temperature for a given Cu_2Te thickness. The increase of CdTe doping concentration with Cu_2Te thickness is less pronounced in the case of the 250ºC deposition, and totally absent in the case of the higher deposition temperature (350ºC). As explained earlier, Cu_2Te deposited at 250ºC is essentially stoichiometric, signifying that there is only a small amount of free copper. Thus the increase in doping in CdTe for higher Cu_2Te thickness is small. However the higher temperature of Cu_2Te deposition, results in Cu rich films. Thus, more Cu is available for diffusion into the CdTe bulk to increase its doping effectively regardless of the thickness. Further, the higher temperature of deposition also aids Cu diffusion and incorporation into the CdTe. The higher doping concentration leads to shrinkage of the depletion region, which could result in poor

carrier collection. Since the doping of CdTe appears to increase, it can be concluded that ZnTe does not prevent or limit Cu diffusion into CdTe. From the preliminary experiments performed above, it seems that the deposition temperature of 250ºC and thickness of 150Å is close to optimum for Cu_2Te deposition when used with ZnTe in a bi-layer structure.

Before further optimization of the contact properties some of the cells used for contact studies were utilized for accelerated stability testing of these contacts.

6.1.3 Stability Studies of ZnTe/Cu_2Te Contacts

In order to study the feasibility of this contact for large scale applications, the cells were subjected to accelerated stress testing. The cells were annealed in N_2 ambient at atmospheric pressure at an elevated temperature of 70ºC. The cells were tested at regular intervals to study the contact properties progressively with time. Table 9 gives the variation of Voc and FF's with time of stress.

Table 9 Variation of V_{oc} and FF with Time of Stress

Time of Stress, (hrs)	V_{oc}, mV	FF, (%)
initial	816	71.4
150	823	69
425	820	53.9
700	831	49.4

From the above table it can be seen that there is a drastic reduction in FF with time of stress although the V_{oc}'s show some improvement. The slight increase of V_{oc}s with time could be attributed to increase in doping concentration in CdTe due to an increase in Cu doping during the temperature stress. However the increase is not very pronounced probably due to the increase in the back barrier with stress time. The loss of fill factor can be explained using figure 29, which provides the I-V curves of the above device at different stress times

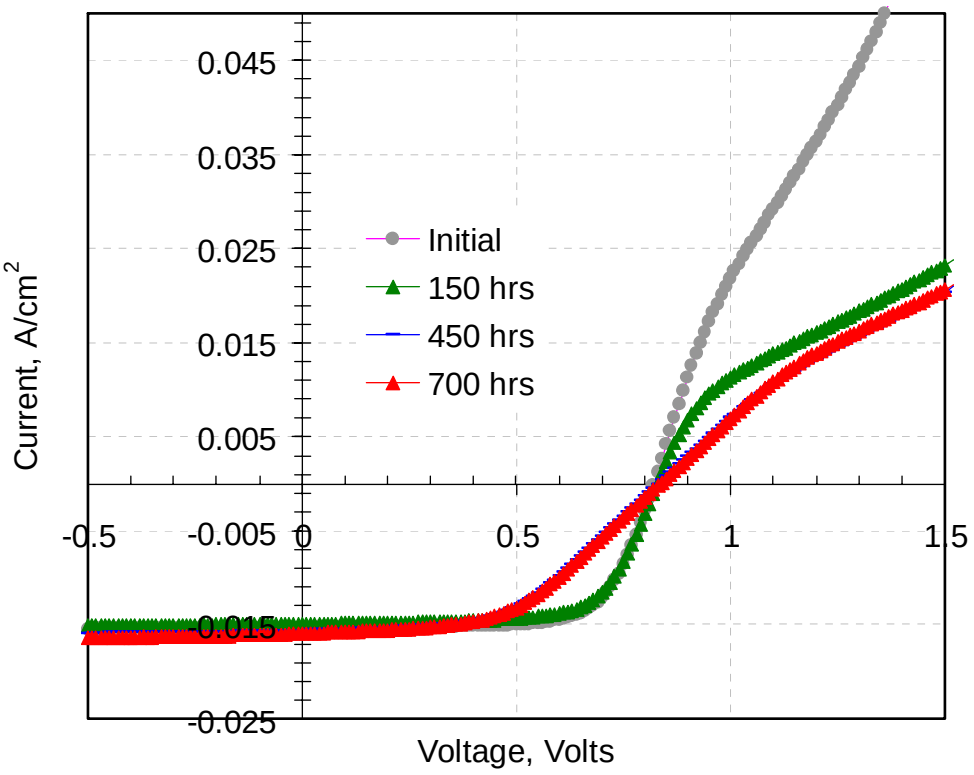


Figure 29 J-V curves of Same Device with Stress Time (70ºC)

The kink observed in all the curves at higher forward bias, suggests that the contact is rectifying. However at lower bias (close to V_{oc}), the presence of a smaller

barrier makes carrier transport easier thereby causing no adverse effects on the fill factor of the device. For stress times beyond 150 hrs the back barrier appears to be relatively constant. The series resistance component (linear term) however increases probably due to Cu diffusion into CdS(making it more resistive) and Cu diffusion from the ZnTe region to the metallurgical junction.

The rate of deterioration of the I-V curve is further increased when the devices are stressed at higher temperature of 100ºC, as shown in figure 30. As is observed from the curves the reduction in fill factor is even greater than in the case of the device stressed at 70ºC. In this case there is also reduction in the short circuit current due to the very high series resistance, most likely caused by the increased diffusion of copper at these temperatures

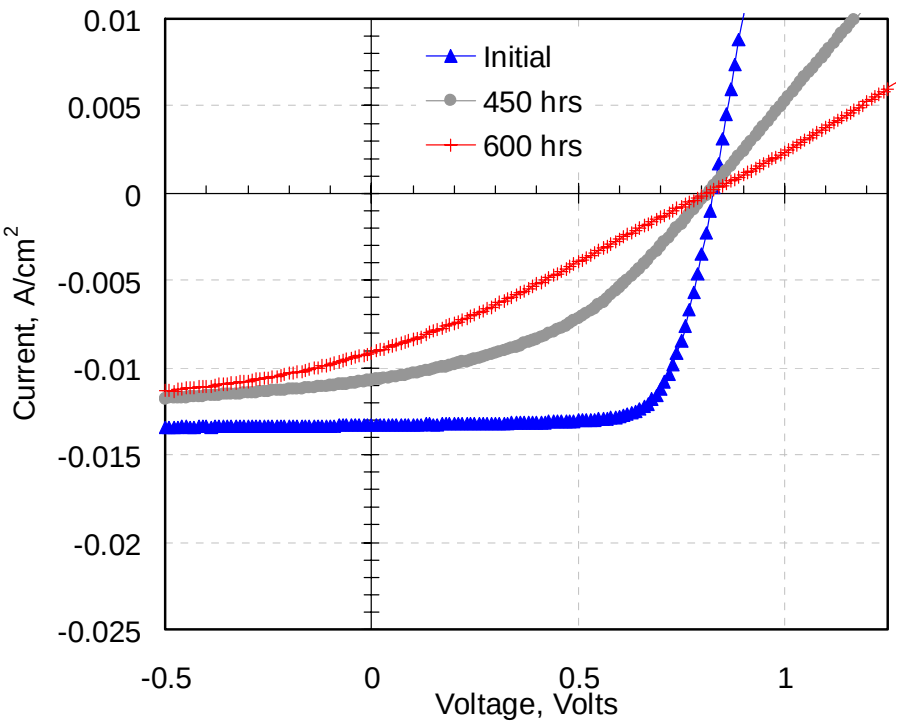


Figure 30 J-V Curves of Same Device with Stress Time (100ºC)

The stability study of the ZnTe/Cu_2Te contact thus suggests that it suffers from problems similar to the Cu contacts, namely, degradation caused by the diffusion of Cu with time away from the back contact region. Thus the focus of this work was directed to finding alternate Cu free strategies

6.2 Sb_2Te_3 Contact

The first attempt to obtain alternatives to copper in back contact applications of CdTe solar cells was the study of Sb_2Te_3. Experiments to determine the suitability of Sb_2Te_3 for contacts to CdTe solar cells were performed by varying the Sb_2Te_3 thickness, and the Sb_2Te_3 deposition temperature. Before the deposition of Sb_2Te_3 on cells, depositions were performed on glass substrates to determine the resistivity and film stoichiometry as a function of the deposition temperature. The resistivity was found to decrease with temperature as summarized in Table 10.

XRD measurements of films deposited on glass at various temperatures are shown in Figure 31. Sb_2Te_3 was found to be present in all films. At low temperatures the films appear more amorphous with the crystallinity improving with the temperature of deposition [44].

Table 10 Resistivity of Sb_2Te_3 as a Function of Deposition Temperature

Deposition Temperature, °C	Resistivity, ohm cm
25	1.6496
200	1.148×10^{-3}
250	1.26×10^{-3}
275	1.088×10^{-3}
300	6.53×10^{-4}
350	9.668×10^{-4}
375	1.413×10^{-4}

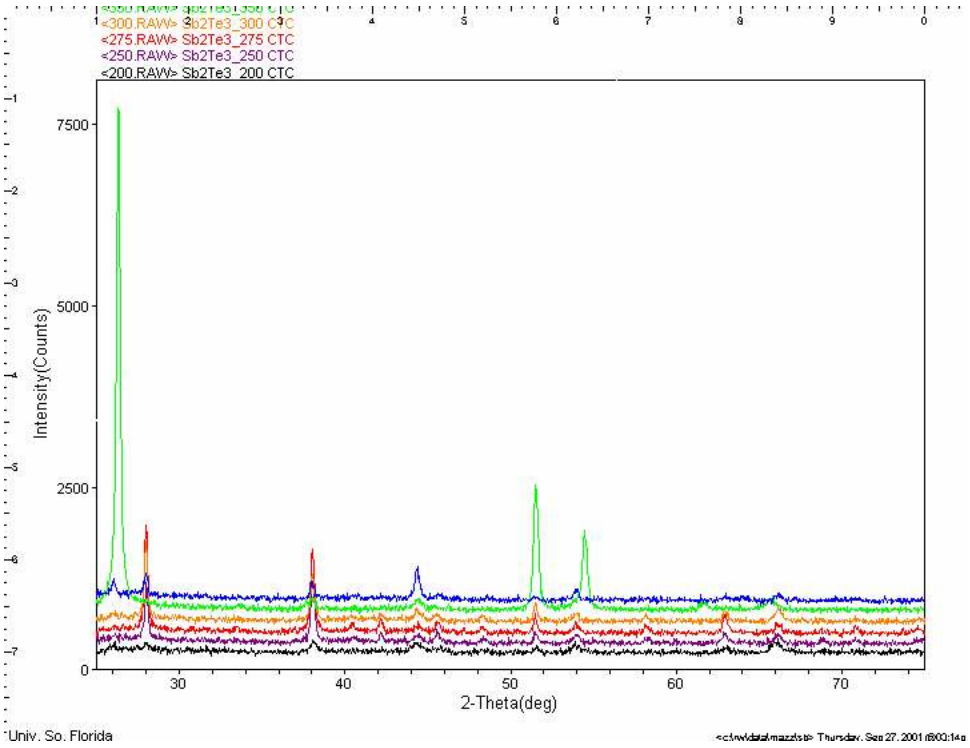


Figure 31 XRD Patterns of Sb_2Te_3 Films at Various Temperatures

6.2.1 Effect of Sb_2Te_3 Deposition Temperature and Thickness

Experiments to optimize contact performance were based on the optimization of Sb_2Te_3 deposition temperature, followed by the optimization of the film thickness. For optimizing the deposition temperature, a constant thickness of Sb_2Te_3 was used (1000Å). The effect of deposition temperature on I-V characteristics is shown in figure 32. It can be seen that the Voc increases with the deposition temperature reaching a maximum at 375ºC, after which there is a slight reduction.

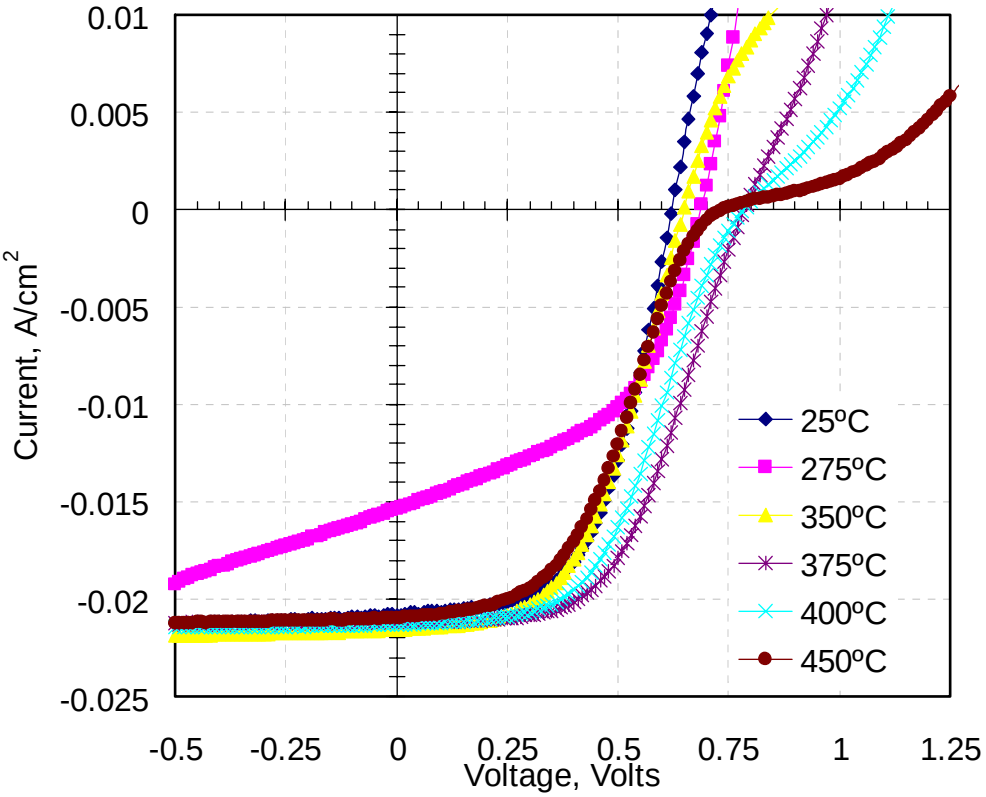


Figure 32 Effect of Sb_2Te_3 Deposition Temperature on J-V Curve

The cause for the observed behavior of V_{oc} is not clear although the low FF seen in all the cells could be attributed to the poor contact as evident from the increased series resistance and rectification observed with increasing deposition temperature.

To determine if the contact properties could be studied further, the thickness of Sb_2Te_3 deposition was varied, while using the optimum deposition temperature derived above. Figure 33 shows the effect of thickness on the device performance. From the I-V curves it can be deduced that although Sb_2Te_3 improves the Voc other device parameters like the FF are much lower than state-of-the-art values. The deposition thickness of 1000Å seems to provide the best results. As was observed in the previous experiment, the FF was affected by series resistance and rectification. No shunting observed in any Sb_2Te_3 contacted cells.

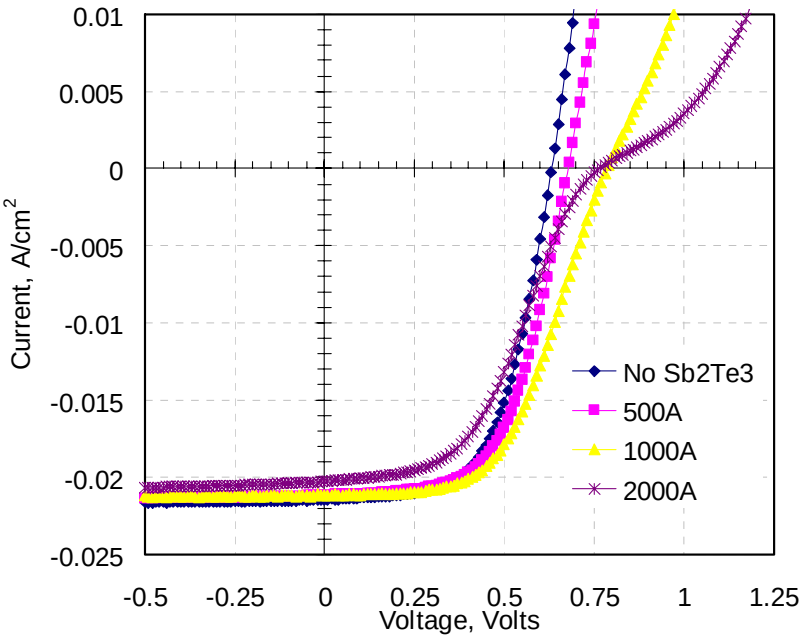


Figure 33 Effect of Sb_2Te_3 Thickness on J-V Characteristics

An interesting observation is that a post-deposition anneal (after the molybdenum deposition) was found to be beneficial for device performance of all cells, in particular the ones with higher Sb_2Te_3 thickness

In order to obtain a better understanding of the effect of Sb_2Te_3, SIMS measurements were performed on the cell with the best solar cell characteristics. The SIMS analysis was performed at the Materials Characterization Facility at UCF [43]. The profile shows the existence of a distinct Sb_2Te_3 layer as evidenced by the increase in the Sb and Te profiles in that region. Also, there appears to be no trace of Sb in the CdTe bulk indicating that the Sb does not diffuse into CdTe to help dope it p-type (at least within the detection limits of this technique). This indicates that the Sb_2Te_3 film is very stable.

Further experiments to improve the performance of the contact did not yield any encouraging results, contributed in part by the difficulty in obtaining repeatable results..

The best individual parameters obtained using the Sb_2Te_3 contact was Voc = 784mV, FF = 59.8%, Jsc = 21.4mA/cm^2 corresponding to an efficiency of 10.07%

6.3 Ni-P Contact

The objective of this study was to determine the feasibility of Ni-P alloys for use as back contacts to CdTe. For this purpose Ni_2P powder was mixed in graphite paste and applied on the etched CdTe surface. The effect of Ni_2P concentration, temperature and time of anneal on device performance was characterized.

6.3.1 Effect of Ni_2P Concentration

The dependence of cell characteristics on the Ni_2P concentration in the graphite paste, was studied using three Ni_2P concentrations (10%, 25%, 40% Ni_2P by wt).

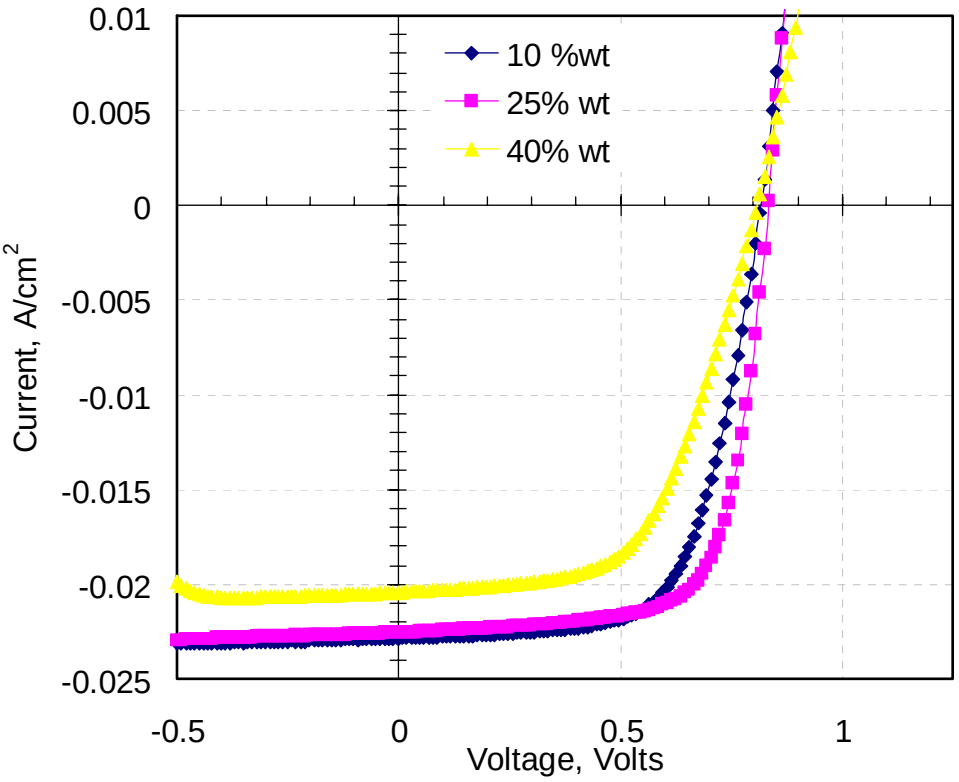


Figure 34 Effect of Ni_2P Concentration on the J-V Curve

The I-V characteristics of CdTe solar cells as a function of the Ni_2P concentration are shown in figure 34. From the figure it can be deduced that a Ni_2P concentration of 25% leads to better device performance. The observed increase in series resistance at concentrations above 25% Ni_2P by wt is due to the onset of rectification. This effect of concentration is not clearly understood at this time, and additional analysis is necessary in order to undesratnd the underlying mechanisms. However, it appears that one of the

reasons for this behavior could be the effect of increasing dopant mixture in the graphite paste on graphite consistency causing poor contact adhesion. For further studies the concentration of 25% has been chosen as the optimum.

6.3.2 Effect of Post-Deposition Anneal Temperature

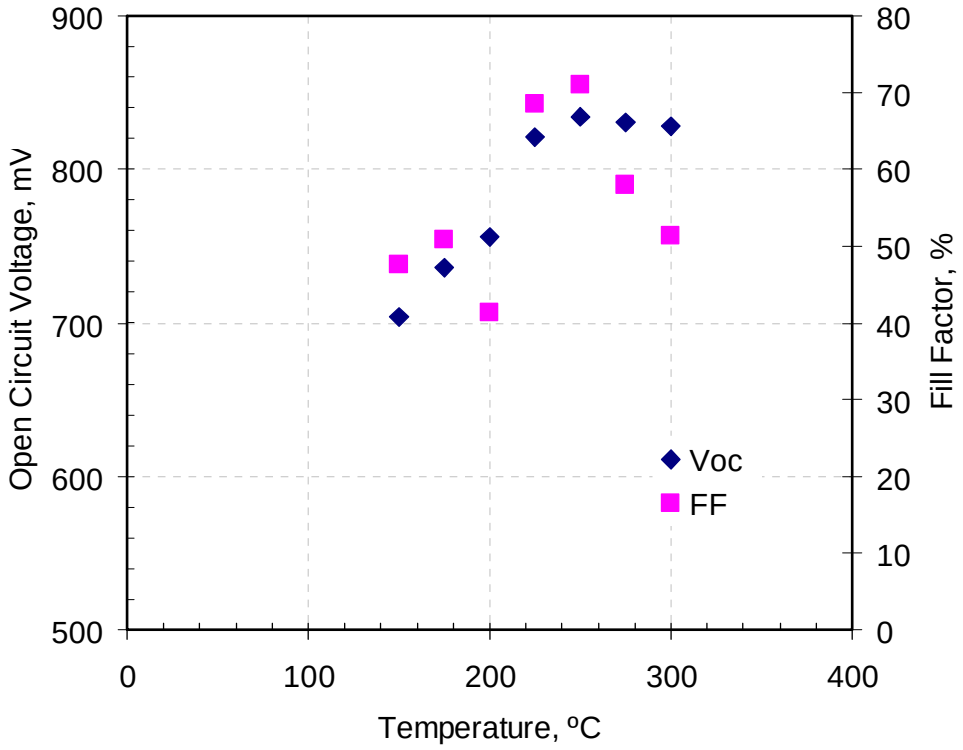


Figure 35 V_{oc} & FF as a Function of Anneal Temperature

After contact application the samples were annealed in an inert ambient (typically He) in the temperature range of 150 – 300ºC. Figure 35 shows the variation of the V_{oc} and FF as a function of annealing temperature. As the graph illustrates the V_{oc}'s and FF's peak at 250ºC. For temperatures above 250ºC the FF appears to decrease. This decrease

in FF is due to the Ni_2P/graphite contacts becoming rectifying for these temperatures. The J-V data in Figure 36 clearly shows that the lower FF's are due to the rectifying back contact.

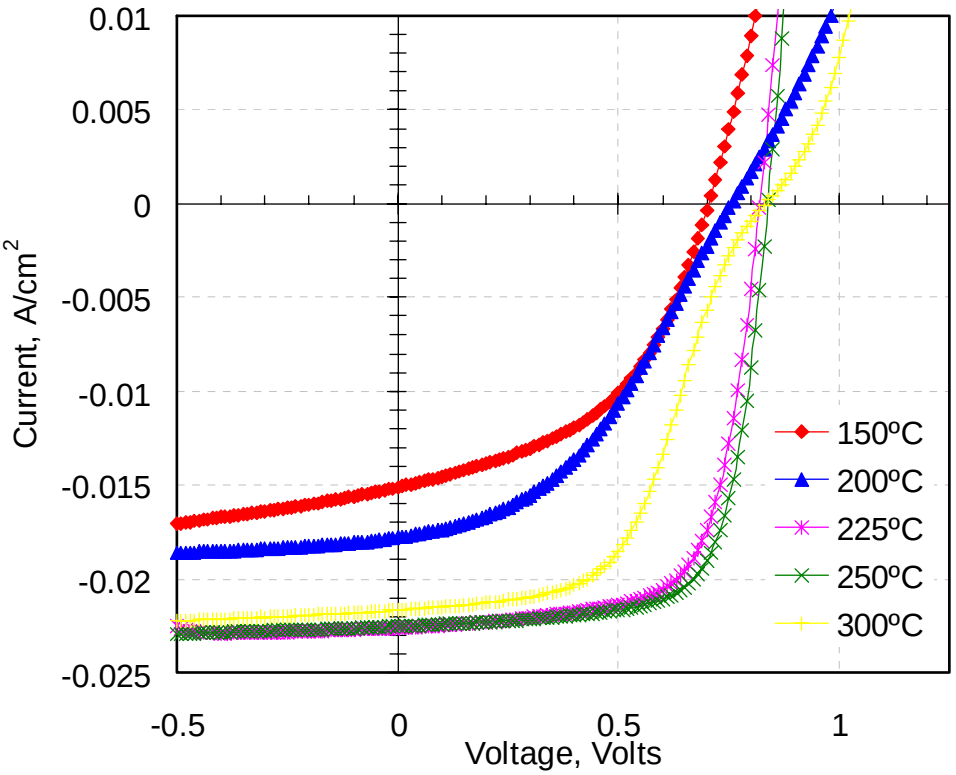


Figure 36 Effect of Contact Annealing Temperature on J-V Curve

The V_{oc}'s and currents decrease at lower temperatures. This is probably due to the poor contact formed at these temperatures suggesting that contact characteristics are strongly affected by temperature. The reasons for the observed behavior are again not clearly understood at this time. However, earlier studies on the Ni-P coatings suggest that the origin of rectification could be attributed to the formation of an unfavorable phase (like Ni_3P) at temperatures above 250ºC. A similar analysis needs to be performed to ascertain that the same phenomenon causes the observed behavior. Attempts to perform

XRD analysis by Brian McCandless at Institute of Energy Conversion (IEC) were unsuccessful due to the overwhelming interference peaks produced by the graphite particles in the contact paste still left on the device even after rigorous cleaning.

6.3.3 Effect of Post-Deposition Anneal Time

In order to determine the effect of annealing time on device performance, several devices were annealed at 250ºC for various anneal times in the range of 15-120 minutes. The dependence of V_{oc} and FF on the post deposition anneal time is summarized in Table 11.

Table 11 Effect of Anneal Time on V_{oc} & FF

Annealing Time, min	V_{oc}, mV	FF, %
15	852	60.9
60	848	63.2
90	850	67.7
120	827	56.7

From the table it can be seen that although the V_{oc} remains essentially unchanged, the FF improves with time up to 90 min after which, it deteriorates. The improvement in FF is due to the reduction in rectification, with time of anneal. C-V measurements, performed on these cells yielded no variation in the doping concentration as a function of time. The results indicate that there is no doping effect of P in the CdTe bulk. Thus the changes observed in the cell behavior could be attributed to the CdTe/contact interface.

The reduction in FF for anneal times above 90 minutes is due to increased series resistance and the onset of rectification, as shown in figure 37. Interpretation of these results would however, again require analysis of the CdTe surface to determine if different phases of material exist for different anneal times.

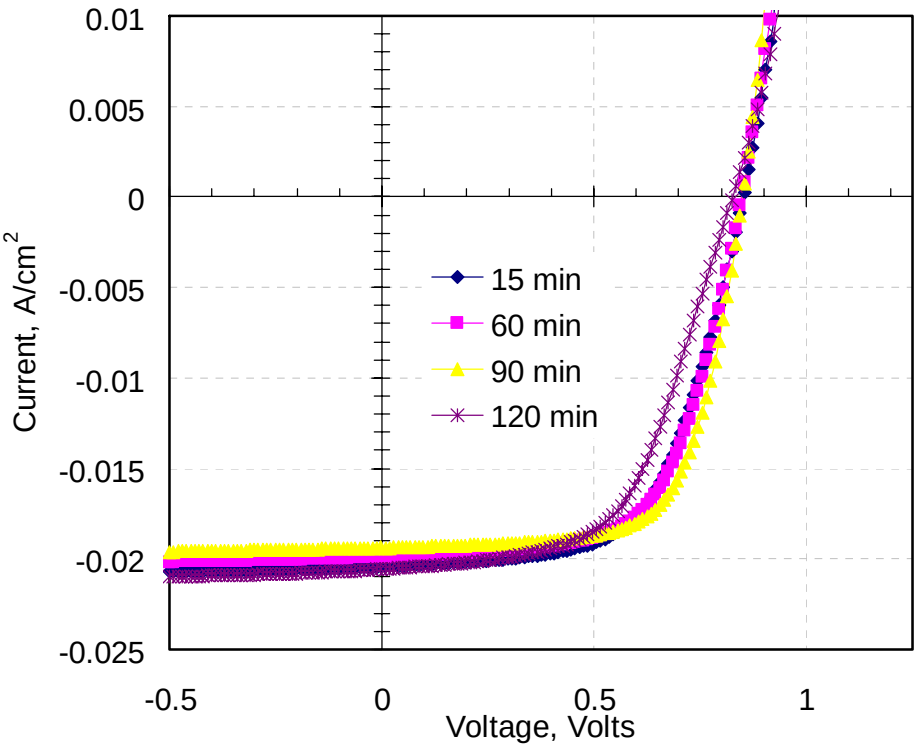


Figure 37 Effect of Annealing Time on Contact Properties

6.3.4 Ni_2P Contact – Characterization

Based on the above-discussed experiments it could be concluded that the contact characteristics are strongly affected by the post-application treatments. However, the reasons for the observed behavior are not yet obvious. In order to explain these behaviors and, in particular the role of nickel and phosphorous in contact formation, SIMS analysis was performed at NREL by Sally Asher.

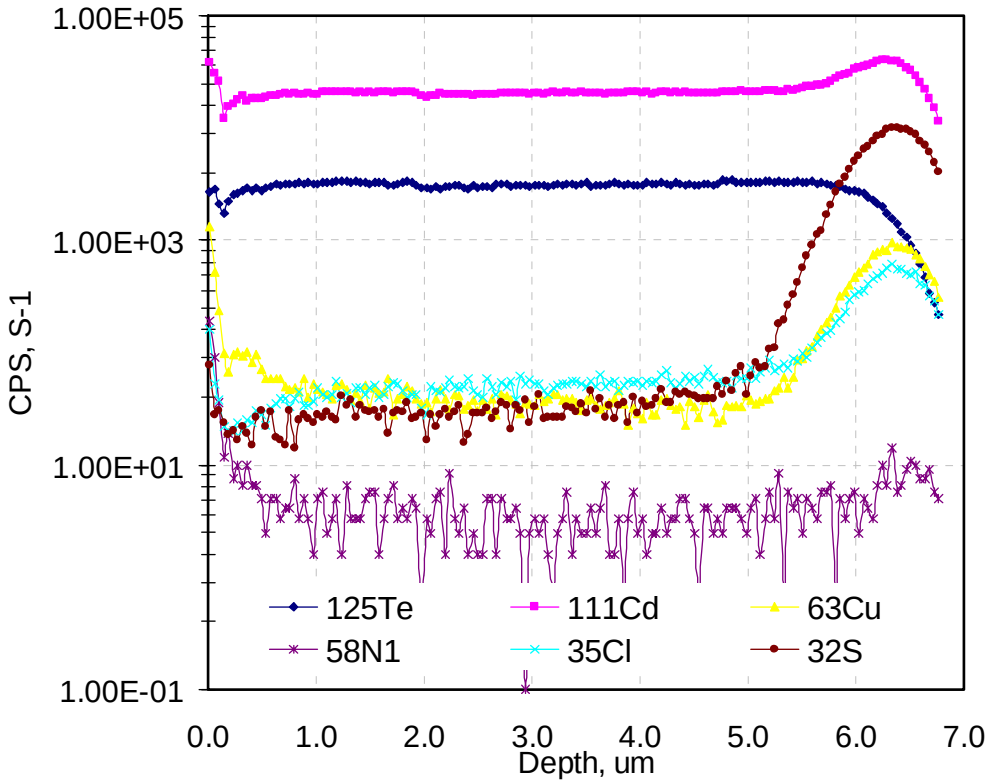


Figure 38 SIMS Depth Profile of a Ni_2P Contacted Cell

The SIMS data was taken with high mass resolution using O_2 primary beam and the detection of positive secondary ions. Figure 38 presents the SIMS depth profile of a CdTe solar cell fabricated at the presently established optimal conditions. Some of the elements like Sn have been removed from the plots for better clarity of the profiles of the elements of interest.

From the profile it is clear that the diffusion of Ni and P in the CdTe is minimal. This indicates that most of the Ni_2P deposited on the CdTe, remains on the surface of the device. This leads to two speculations for contact formation. First, it provides indication that there is a compound of Ni-P formed at the back surface, which probably helps

contact formation. Second, the phosphorous from the Ni_2P probably dopes the CdTe near the back surface highly p-type, while the Ni forms the required final metal (work function ~ 5.1eV). However, conclusive evidence can only be obtained by XRD analysis of the CdTe surface.

Another interesting observation from the SIMS profile is the presence of Cu observed in the CdTe bulk. The source of this copper is probably the graphite paste itself. However, the Cu levels observed in this device are about an order of magnitude lower than that found in cells fabricated using Cu contacts. This was verified by obtaining a SIMS profile of a device fabricated using Cu back contacts. The result of this profiling is shown in figure 39.

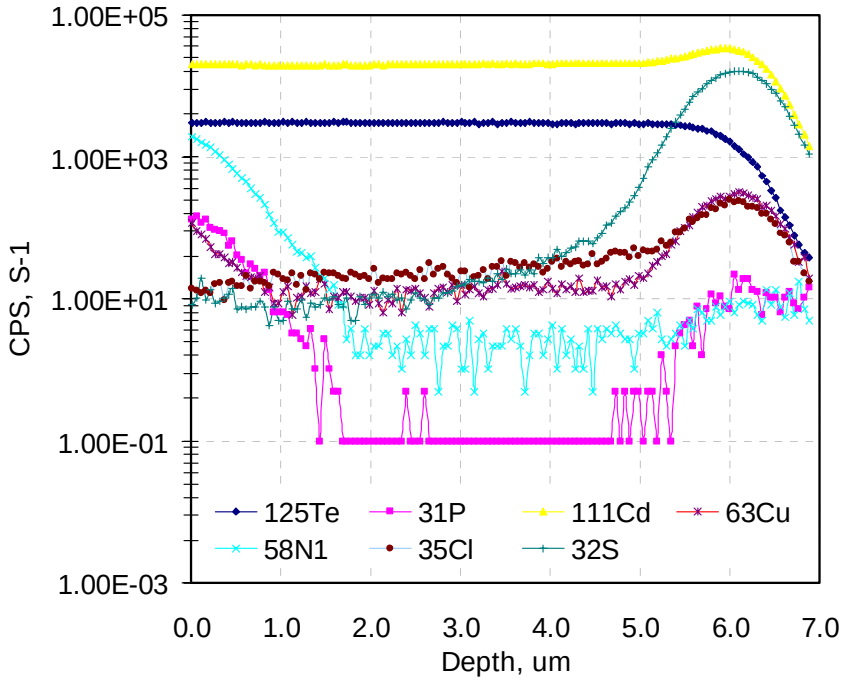


Figure 39 SIMS Depth Profile of a Cu Contacted Cell

As is evident from the depth profile the Cu content at the CdTe back surface is indeed about an order of magnitude higher than that found in the Ni_2P contact. Thus the profiles of both the Ni_2P and the Cu contacted cells validate the fact that the Ni_2P present in the graphite is indeed responsible for the observed contact characteristics presented earlier.

6.3.5 Stability

Based of the result of the above experiments Ni_2P proved quite effective for use as back contact material in commercial solar cells. A particular advantage of this contact is probably the reduced diffusion of P in the CdTe, which could indicate that the contact could be quite stable. Thus, one of the most important issues that need to be addressed for the use of Ni_2P contacts in large-scale production is related to the stability of the contact. Initial study of the Ni_2P contact was performed by annealing the contact at 70ºC in an inert ambient. The performance of the device was then evaluated progressively up to 1000 hours. A comparison of the variation of V_{oc} and FF with stress time (up to about 1000 hours) is illustrated in Table 12.

Table 12 Variation of V_{oc} & FF of Ni_2P Contacts Annealed at 70ºC for 1000hrs

Time, Hrs	Open Circuit Voltage, mV	Fill Factor, FF,%
0	851	67.6
400	832	66.7
600	830	65.9
800	833	65.0
1000	832	63.1

From the above table it can be seen although the reduction is minimal, the reduction in FF is more pronounced than the loss of V_{oc}.

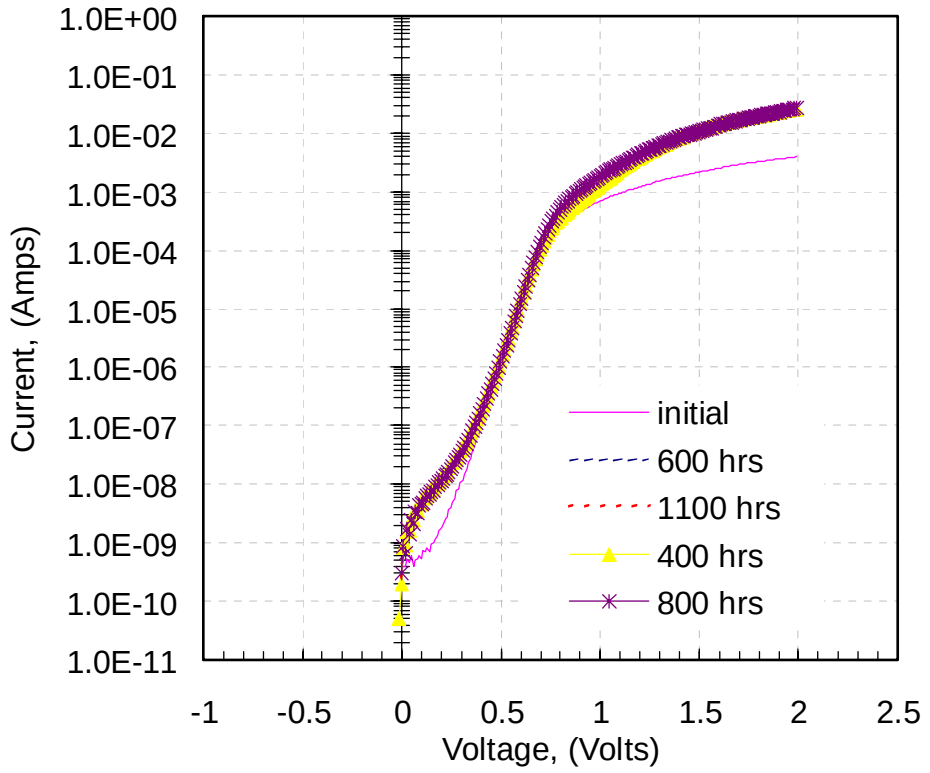


Figure 40 Dark J-V curve of Stressed Devices at Various Stress Times

In addition, the loss in V_{oc} occurs in the first 400 hrs and stabilizes with further stress on the device. The loss in V_{oc} is not understood as the dark JV curves, shown in figure 40, at the different stress times does not show the observed behavior clearly, although from the point of view of this experiment it can be concluded that the loss of V_{oc} is not the effect of change in contact property with stress.

Another important observation in the case of the stress test on the Ni_2P contact is the absence of any rectification with the stress, shown in figure 41.

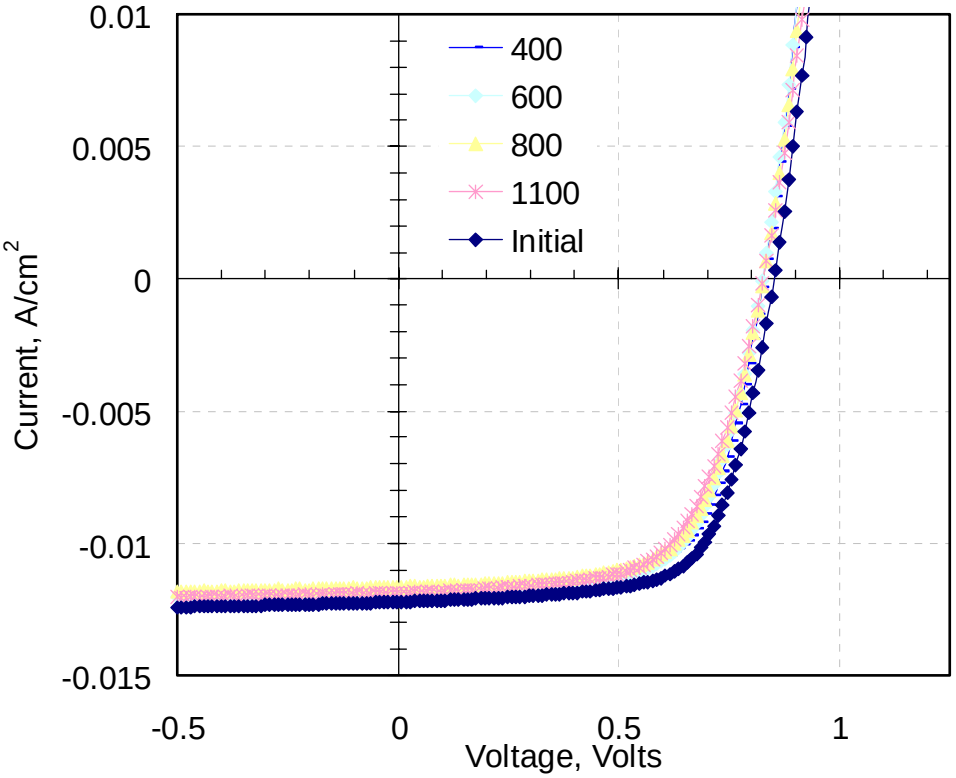


Figure 41 Light I-V Curve of the Same Device at Various Stress Times

This is in sharp contrast to that observed in the Cu_2Te and the $ZnTe/Cu_2Te$ contacts. This shows that the contact properties are quite stable and thus Ni_2P could serve as the preferred contact for CdTe solar cells in commercial applications.

The best cell fabricated to-date using the Ni-P contact had a V_{oc} = 833mV, Jsc = 20.34 mA/cm2, and a fill factor = 70.7% corresponding to an efficiency of 12%. The low J_{sc}'s observed in this devices(I-V shown in figure 42) is expected because the CdS

window layer was made intentionally thick to remove shunting effects caused by thin CdS. An optimized CdS layer would thus help boost these efficiencies further.

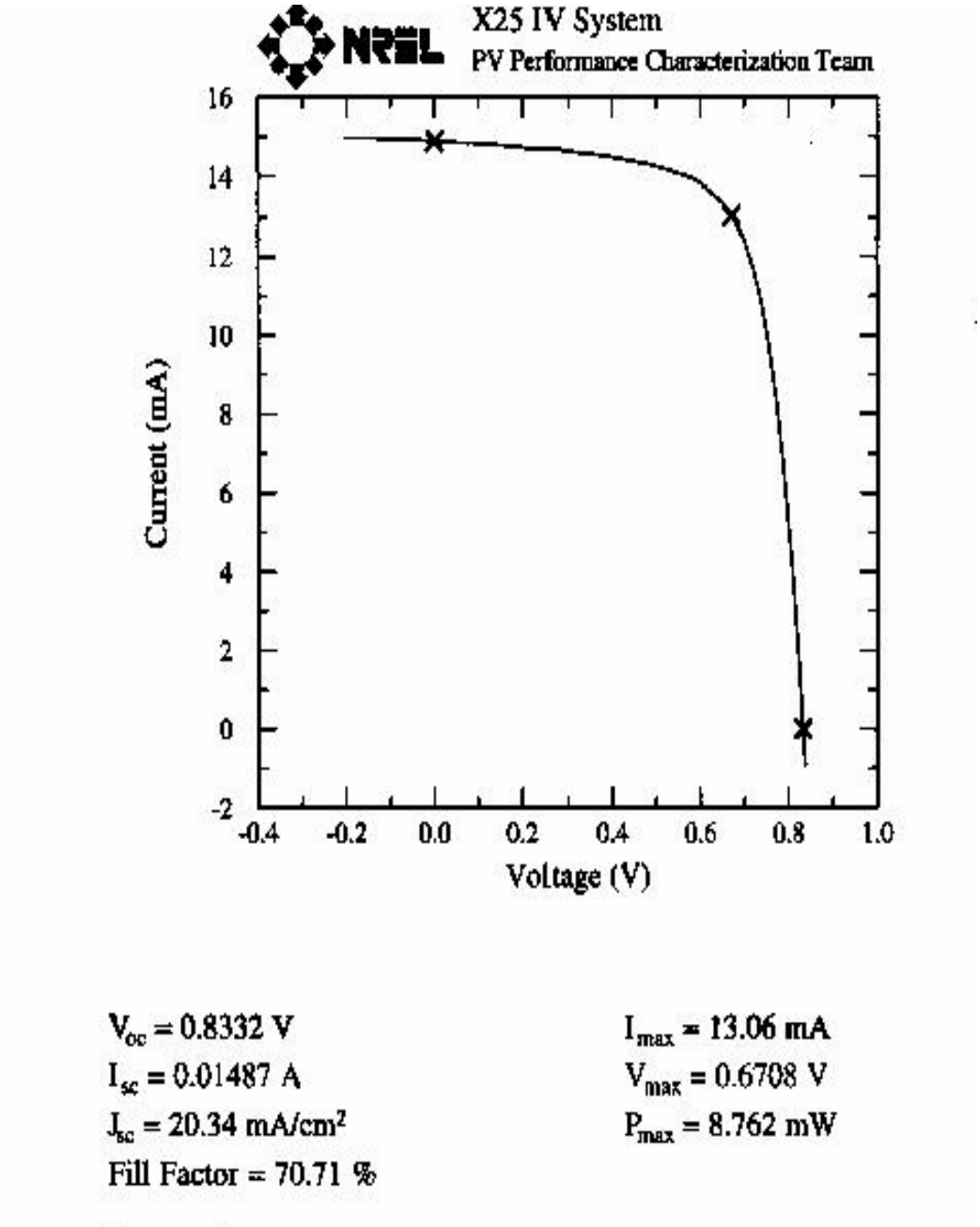


Figure 42 I-V Curve of the Best Device Measured at NREL

Although these results look encouraging its important to realize that further characterization is necessary to understand and study the actual mechanism of the contact. This in turn would help optimize contact properties to improve efficiency and reliability.

6.4 Dry Etch for Back Contact Formation

Typically CdTe solar cells use wet etching techniques for surface preparation prior to back contact formation predominantly. This, however, is undesirable due to the reduced control obtainable using wet chemistry for removing a few monolayers. In addition, the formation of oxide after the etching process helps to diminish the purpose of etching. Thus a better approach would involve a dry etch process which could be better integrated to provide an all-vacuum process for CdTe solar cell manufacture. This work explores the use of a dry etching process for polycrystalline solar cell fabrication. The etchants used in this study were Ar, N_2 and O_2. The cell characteristics were studied as a function of plasma power, pressure, and time of etch. Graphite paste doped with HgTe:Cu was used as back contact for these devices after the etching process.

6.4.1 Effect of Plasma Power on Cell Performance

Initial studies were conducted in N_2 gas by varying the etch power and time, keeping the chamber pressure constant at 250mT. The effect of these parameters on the Voc and FF is shown in figures 43 & 44.

From figure 43 it is evident that the plasma power of 50W provides the highest Voc's and progressively decreases as the power is increased. The Voc is also influenced

by the etch time, in that at lower power it improves with time reaching a maximum for 10-15 min etch time. At higher powers (above 50W) it deteriorates with the time of etch.

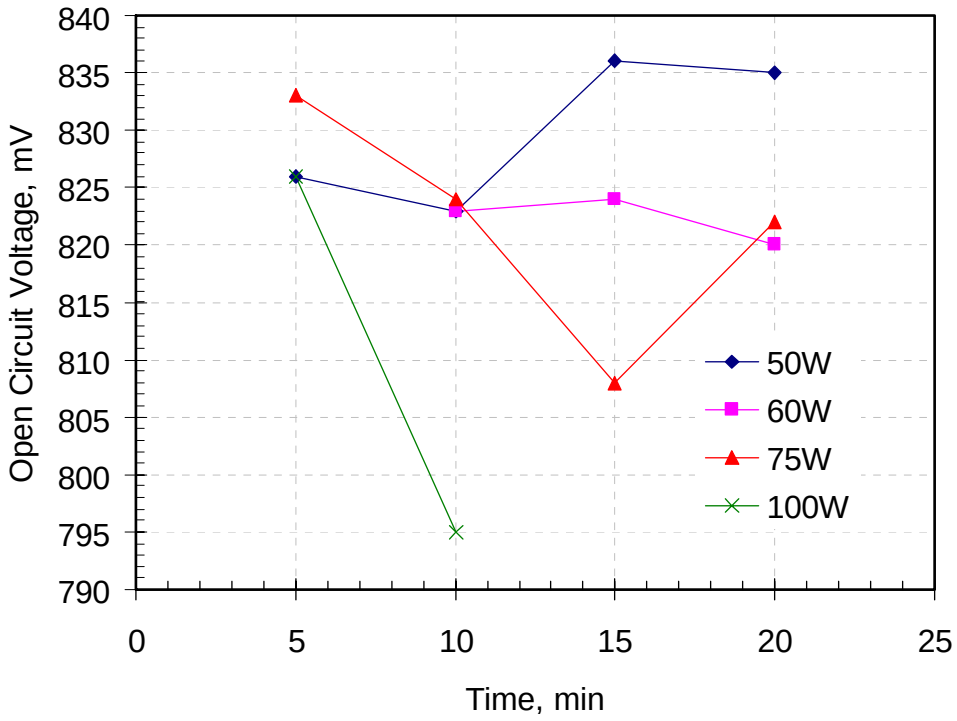


Figure 43 Effect of Plasma Power on V_{oc}

The effect of sputter power on the FF was found to be similar to that of Voc, indicating that the observed behavior is a reflection of the contact formed. This behavior is illustrated by comparing the effect of etching time at 50W and 75W on the I-V characteristics of the solar cells. The improvement in FF initially with the etch time, in the case of the 50W and 75W etch, is the improved contact formation with time. The reduction in the FF is due to the onset of rectification clearly observed in the I-V curves of figure 45 as we move away from the optimum time of 10-15 min (50W plasma power).

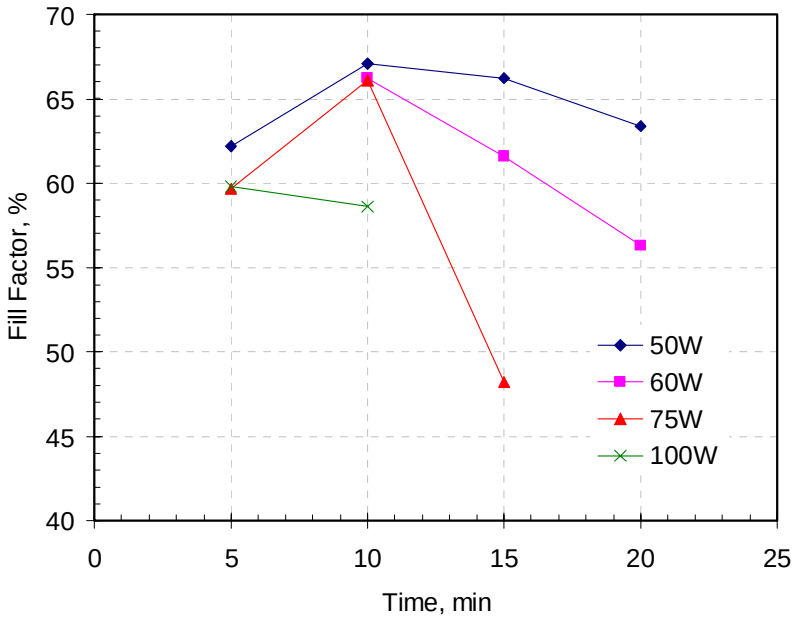


Figure 44 Effect of Plasma Power on FF

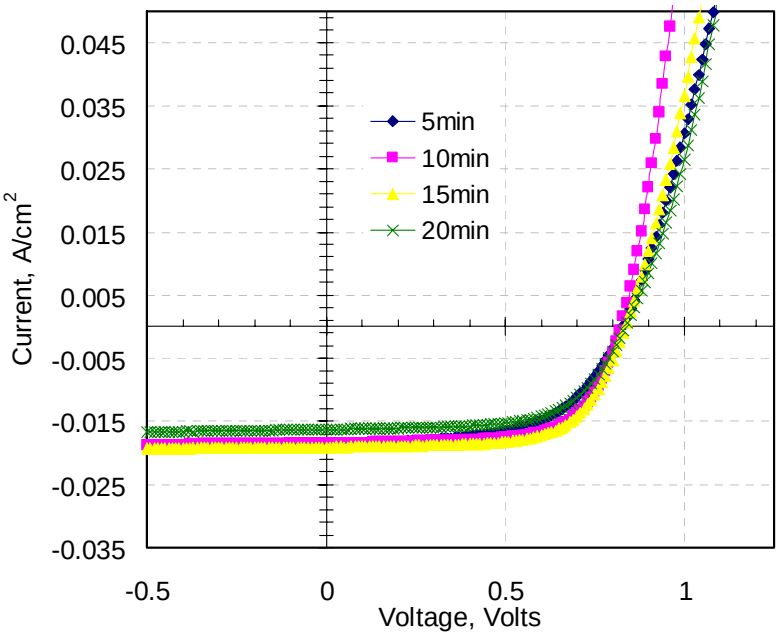


Figure 45 Effect of Plasma Etch Time on J-V Characteristics(50W)

As is the case in most materials, a thin layer of oxide ($CdTeO_3$) is known to form on the surface of CdTe on exposure to O_2. The contact formed on such a surface is rectifying leading to low FFs. The improvement of FF in the plasma-etched devices could be attributed to the removal of this layer by the etching process. In addition, based on previous work done by S.Gurumurthy et al[45], a tellurium rich layer is created as a result of the etching process in N_2. The rectifying properties observed for longer etch times however are probably caused by the plasma induced damage of the surface which could lead to the formation of defect states at the CdTe/contact interface in turn causing a reduction in carrier collection at the contact-CdTe interface. This leads to reduced FF and V_{oc} as can be seen from the above graphs.

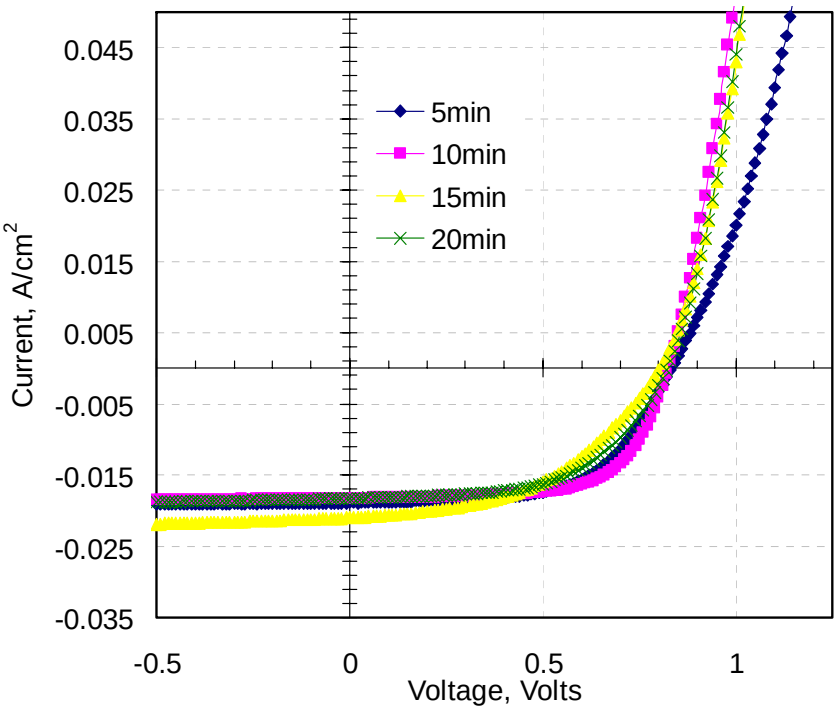


Figure 46 Effect of Plasma Power of 75 W on the J-V Characteristics

Further, it can be observed that the deterioration of FF with time is more pronounced for higher power providing further evidence on possible plasma damage. In the case where the samples were etched at 75W(figure 46) the optimum etch time is shorter than that at 50W possibly due to the higher rate of removal of surface oxide by the higher plasma power. In this case the optimum time is clearly 10min. The rectification observed at 75W is also found to be more pronounced.

6.4.2 Effect of N_2 Gas Pressure

The effect of plasma pressure on the contact properties was studied in the pressure range of 150-400mT, keeping the etch power constant at 50W. The effect of pressure on the properties of the solar cells is tabulated below

Table 13 Effect of N_2 Pressure on Device Properties

Sample #	Etch Pressure, mT	V_{oc}, (mV)	FF, (%)
11-11b-8a3b	150	831	60.6
11-11b-8a4a	200	826	61.6
11-11a-8a1a	250	823	67.1
11-11a-8a2a	300	819	66.5
11-11a-8a4a	400	814	56.8

From the table above it could be deduced that the V_{oc}'s remain essentially unchanged except at 400mT where a slight reduction can be observed (comparing same sample #'s). The cause for the observed decrease can be deduced using the comparison of

light I-V curves of devices etched at 250, 300 and 400mT in figure 47. It can be seen that the slight reduction in the V_{oc} and the greater reduction in FF of the device etched at 400mT is due to the reduced carrier collection which in-turn causes a soft knee to the I-V curve.

For a given power applied to the electrodes the pressure in the chamber influences the energy associated with the process. Beyond a certain critical pressure, in a low pressure regime the ions that impinge the surface have greater energy than they would at

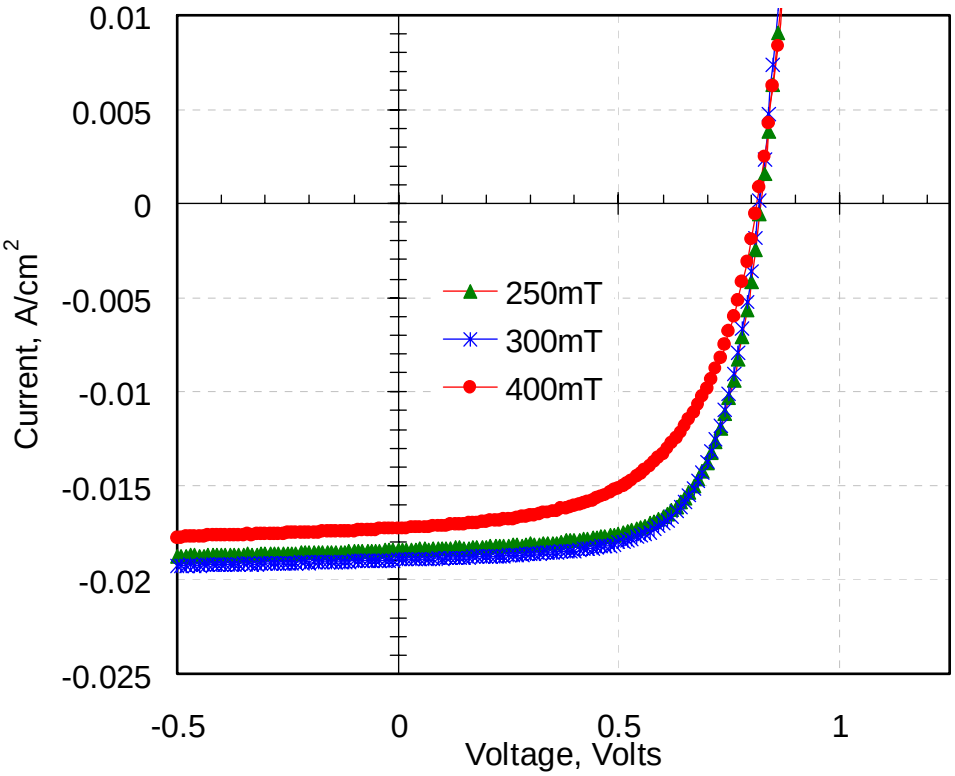


Figure 47 Effect of Pressure on Cell Performance

higher pressure. This is due to the reduction in collision frequency, which causes loss of energy of the ion. The result of this phenomenon is that the etching efficiency is increased. On the contrary, higher energy of the impinging ions can also cause lattice

damage, which could lead to formation of recombination centers that affect carrier transport across the back contact. Based on the above experiment, it appears that the pressure of 250mT seems to provide the best compromise.

Thus, the initial studies on dry etching of CdTe using N_2 have been successful. The optimized process at this point uses an etch power of 50W for 10min in 250mT of N_2.

6.4.3 Dry Etching in Argon

In order to obtain a better understanding of the mechanism of the etching process and the effect of N_2, experiments were performed using Ar. The behavior of the devices under inert etching conditions could provide insight, in that, it could help determine if the desired improvements were a result of a mechanical, chemical or a combination of both processes.

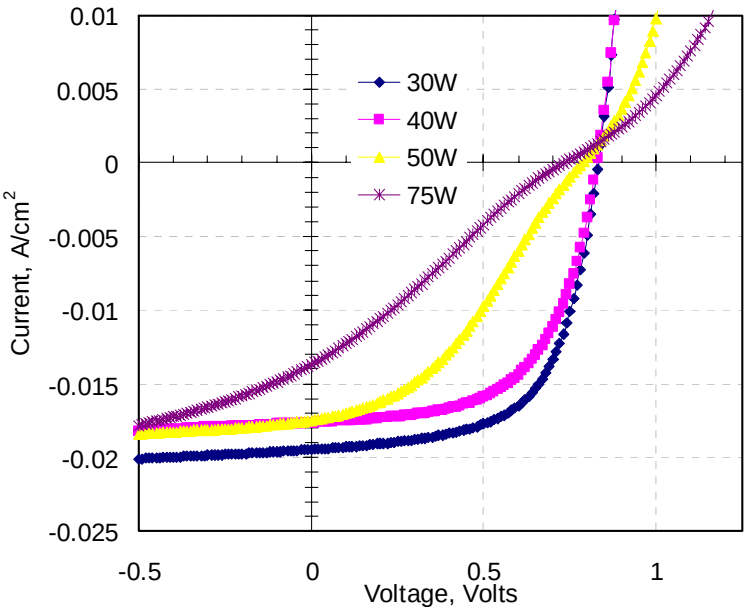


Figure 48 Effect of Plasma Power on J-V Curve using Ar as the Etching Ambient

Figure 48 shows the variation of cell characteristics with the power used for the etching process. The pressure was kept constant at 250mT. It can be observed that the J-V curve improves as the power is reduced, reaching a maximum at 30W. This is primarily due to the improved contact characteristics, which is initially rectifying at 75W and becoming more ohmic as the power decreases. The improvement in the contact properties at lower powers is attributed to the possible reduction of plasma damage. Argon is a heavy atom and hence more effective than N_2 (a lighter atom) in causing damage to the CdTe lattice. This explains the shift to lower energies of the optimum condition in the case of etching using Ar. Experiments to study the effect of further reduction in plasma etch power could not be done because of the difficulty in sustaining the plasma at low powers.

Based on this study it appears that the observed improvement in contact properties is due to removal of a surface oxide layer by the process of sputter etching.

In order to confirm this hypothesis, the surface etching was performed in a mixture of N_2 and O_2 keeping the total pressure constant at 250mT. This was done by first setting the N_2 flow to the desired level, followed by adjusting the O_2 flow meter to read a total pressure of 250mT.

The effect of adding O_2 to the etching environment is quite clear from the above table. The FF is drastically affected although the change in Voc is within experimental variation. This suggests an degradation of contact properties in the presence of O_2 in the chamber. This is shown in figure 49.

Table 14 Effect of N_2:O_2 Ambient on Device Parametrics

N_2:O_2, (mT)	V_{oc}, (mV)	FF, (%)
250:0	830	64
240:10	831	56
225:25	839	45.5
200:50	836	30

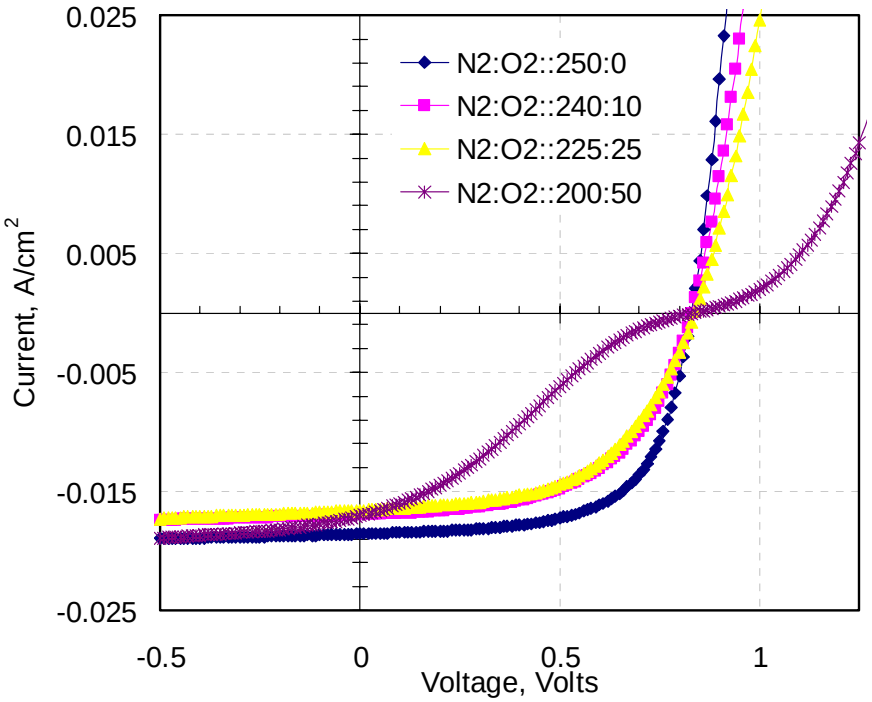


Figure 49 Effect of Increased O_2 Partial Pressure on J-V Characteristics

The sputtering of the surface oxide on the CdTe surface by the plasma process is partially negated by trace amounts of O_2 present in the ambient. Oxygen in trace amounts can cause oxidation of the CdTe surface formed by the etching process. The oxidation

process is probably enhanced by virtue of the fact that the O_2 atoms are probably in a more excited state and hence bond easily bond to the CdTe surface. This explains the degraded contact properties with increased amounts of O_2 in the etching ambient.

Based on the experiments performed on this study it can be concluded that the dry etching of the CdTe surface for contact formation can be applied successfully for CdTe solar cell fabrication. The process of dry etching is favorable since it lends itself more suitable for large scale manufacture of these devices. The ambient gases, namely Ar and N_2, are both suitable for the sputter etching process. The impinging ions help remove surface oxides in CdTe thereby helping contact formation. The presence of any trace amounts of O_2 is found to be detrimental to the etching process and needs to be avoided. The complete benefit of the dry etching process can be obtained by using back contact methodologies that can be done in vacuum to minimize the exposure of the CdTe surface to the atmosphere after etching.

CHAPTER 7

CONCLUSIONS

The primary objective of this work was to explore copper-free alternatives for back contacts to polycrystalline CdTe solar cells. The materials researched for this purpose were Sb_2Te_3 and Ni-P alloy. However, before focusing on Cu-free alternatives, considerable work was done to determine the suitability of ZnTe/Cu_2Te contacts. The effect of Cu_2Te thickness, and anneal temperature on device characteristics were studied. Although devices with good characteristics were routinely obtained in this work, reliability studies indicate a marked degradation in contact characteristics with time of stress. It appears that the ZnTe layer is incapable of limiting the diffusion of excess Cu toward the junction, which leads to the observed device deterioration.

The study of Sb_2Te_3 did not lead to any good results due to rectifying nature of these contacts. In addition, the results were confounded due to the inability to obtain repeatable performance probably due to problems with reliable film deposition. The best individual parameters obtained using the Sb_2Te_3 contact was V_{oc} = 784mV, FF = 59.8%, Jsc = 21.4mA/cm^2 corresponding to an efficiency of 10.07%.

The work on Ni-P(mixed in graphite paste) contact provided very encouraging results. The effect of Ni_2P concentration, annealing temperature, and time on cell performance was studied. The conclusions derived from these studies indicate that the

annealing temperature of 250ºC is critical for good contact performance. Beyond this temperature there is significant rectification observed, pointing to the possibility of change in phase (from Ni_2P to Ni_3P) of the Ni-P material as published elsewhere []. This behavior could however not be verified due to the limitations of characterization facilities available at the time of this study. The reliability of the Ni-P contact was also explored by temperature stressing of these devices in excess of 1000 hrs. The degradation in FF (about 6.6%) although minimal was more pronounced than V_{oc}(2.2%). It is quite encouraging to note that unlike Copper contacts no rectification was observed with stress time, showing that the contact is quite stable. A more thorough study of the contact mechanism will further help optimize performance and reliability. The best device measured at NREL had a V_{oc} = 833mV, Jsc = 20.34 mA/cm2, and a fill factor = 70.7% corresponding to an efficiency of 12%.

Dry Etching of CdTe was also studied as an attempt at a more manufacture friendly process solution for CdTe solar cells. The effect of N_2, Ar and O_2 on contact performance as studied. The results of these studies indicate that the etch process is mechanical in nature where the surface oxide is removed by the sputter etching. The etching mechanism is more pronounced with Ar(being the bigger element) although the use of N_2 has interesting possibilities of also doping the CdTe favorably. Trace amounts of O_2 added to the etching ambient results in poor performance possibly due to re-oxidation of the etched surface. Further characterization of the etching process will help optimize cell performance and eventually replace the wet etching processes currently being employed in these devices.

REFERENCES

1. H.J. Hovel, Semiconductors and Semi-metals, Academic Press, NewYork, 1975.

2. C.S. Ferekides, and J. Britt, Solar Energy Materials and Solar Cells, 35 (1994), 255.

3. E.H. Rhoderick, Metal Semiconductor Contacts, Oxford University Press, NewYork, 1988.

4. G.W. Neudeck, P-N Junction Devices, Addison Wesley, 1989.

5. H.J. Moller, Semiconductors for Solar Cells, Artech House, Boston, USA, 1993.

6. D.M. Oman, K.M. Dugan, J.L. Killian, V. Ceekala, C.S. Ferekides and D.L. Morel, Solar Energy Materials and Solar Cells,, 58, (1999), 361.

7. A.L. Fahrenbruch and R.H. Bube, Fundamentals of Solar Cells, Academic Press, NewYork, 1983.

8. K.M. Dugan, Masters Thesis, Elect. Engg, University of South Florida, USA, 1995.

9. R. Swaminathan, Masters thesis, Elect. Engg, University Of South Florida, USA, 1994.

10. T.C. Anthony, J. Of Appl. Phys., 5 (1985), 1349.

11. T.L. Chu, S.S. Chu, Progress in Photovoltaics res. Appl., 1, (1993) 31.

12. B.R. Tetali, Masters thesis, Elect. Engg, University of South Florida, USA, 1996.

13. E. Janik, R. Triboulet, J. of Physics D: Appl. Phys, 16(1983) 2333.

14. CRC Handbook of Chemistry and Physics, CRC Press, Cleveland, Ohio, (1977).

15. A.L. Fahrenbruch, Solar Cells, 21, (1987), 399.

16. T.C. Anthony, A.L. Fahrenbruch, J. Appl. Phys., 5, (1985), 400.

17. T.L. Chu, S.S. Chu, K.D. Han, Y.X. Han, Y.H. Hiu, M.K. Mantravadi, Solar Cells, 24, (1988), 27.

18. T.L. Chu, S.S. Chu, C. Ferekides, J. britt, C.Q. Wu, G. Chen, N. Schultz, Solar Cells, 30, (1991), 123.

19. H.C. Chou, A. Rohatgi, J. Electtrochem. Soc, 142, (1995), 254.

20. H.C. Chou, A. Rohatgi, N.M. Jokerst, E.W. Thomas, and S. Kamra, J. Elect. Mat., 25, (1996), 1093.

21. Chun-Teh Lee, R.H. Bube, J. Appl. Phys., 54, (1983), 7041.

22. T.A.Gessert, A.R. Mason, R.C. Reedy, J. Elect. Mat., 24, (1995), 1443.

23. J. Tang, D. Mao, T.R. Ohno, V. Kaydanov, and J.U. trefny, 26th IEEE Photovoltaic Spec. Conf., Anaheim, CA, Sept 30-Oct 3, (1997), 439.

24. T.A. Gessert, P. Sheldon, X. Li, D. Dunlavy, D. Niles, 26th IEEE Photovoltaic Spec. Conf., Anaheim, CA, Sept 30-Oct 3, (1997), 419.

25. J. Tang, D. Mao, L. Feng, W. Song, J.U. trefny, 25th IEEE Photovoltaic Spec. Conf., May 13-17 Washington D.C USA, (1996), 925.

26. E. Janik, R. Triboulet, J. of Physics D: Appl. Phys, 16(1983) 2333.

27. G. Asa, Y. Nemirovsky, J. Appl. Phys., 77, (1995), 4417.

28. T.L. Chu, S.S. Chu, K.D. Han, M. Mantravadi, 20th IEEE Photovoltaic Spec. Conf., (1988), 1422.

29. T.L. Chu, S.S. Chu, Solid-State Elect., 38, (1995), 533.

30. Britt, J., Ferekides, C.S., Appl. Phy. Lett., 62, (1993), 2851.

31. McCandless, B.E, Y. Qu, R.W. Birkmire, First World Conf. Photovoltaic Energy, Conf., Hawaii, Dec 5-9, (1994), 107.

32. V. Viswanathan, Masters thesis, Elect. Engg, University of South Florida, USA, 1997.

33. C.S. Ferekides, V.Viswanathan, D.L. Morel, 26th IEEE Photovoltaic Spec. Conf., (1997), 423.

34. B.Ghosh, S. Purakayastha, P.K. Datta, R.W. Miles, M.J. Carter, R. Hill, Semicond. Sci. Tech., 10 (1995), 71-76.

35. R.W. Miles, B. Ghosh, S. Duke, J.R. Bates, M.J. Carter, P.K.Datta and R. Hill, Journal Of Crystal Growth, 161 (1996), 148.

36. Z.S. El Mandouh, Journal of Material Science, 30, (1995), 1273.

37. B. Roy, B.R. Chakraborty, R. Bhattacharya, A.K. Dutta, Solid State Comm., 25, (1978), 617.

38. N. Romeo, A. Bosio, R. Tedeschi, V. Canevari, Thin Solid Films, 361, (2000), 327.

39. T. Schmidt, K. Durose, C. Rothenhausler, M. Lerch, Thin Solid Films, 361, (2000), 383.

40. D. Levi, D. Albin, D. King, Prog. in Photovoltaic Res. and Appl., 8, (2000), 591.

41. M. Ritala, J. Sarlund, M. Leskela, E. Siponmaa, R. Zilliacus, Solar Energy Materials & Solar Cells, 44, (1996), 177.

42. W.J. Danaher, L.E. Lyons, M. Marychurch, G. C. Morris, Appd. Surface Science, 27, (1986), 338.

43. R. Mamazza, Ph.D, Elect. Engg, University of South Florida, Tampa ,USA.

44. S. Gurumurthy, H. L. Bhat, and Vikram Kumar, Semicond. Sci. Tech., 14, (1999), 909.

ABOUT THE AUTHOR

Vijay Viswanathan received his BS degree in Electronics and Communications Engineering at Sri Venkateswara College of Engineering, University of Madras, and MS degree in Electrical Engineering from the University of South Florida. His master thesis was titled "RF Sputtered Back Contacts To Thin Film CdTe Solar Cells",

In fall of 1997, Vijay joined the Ph.D. program at University of South Florida, under the supervision of Dr. Chris Ferekides, and in 1999 was admitted to the Ph.D. candidacy