Vapor CdCl₂ Processing of CdTe Solar Cells

By

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DEDICATION

To my family
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Polycrystalline CdS/CdTe thin film solar cells are among the leading candidates for low-cost, large scale terrestrial photovoltaic applications. CdTe has a high absorption coefficient and it can absorb the radiant energy within less than 2 µm of thickness. This makes it suitable for thin film applications. CdTe has a band gap of 1.45 eV at room temperature, which is nearly optimum for photovoltaic conversion efficiency under the AM 1.5 solar spectrum. The theoretical maximum efficiency for CdTe solar cells is 29%. However, to-date the experimental value is in the 16 % range.

In most cases CdTe cells are subjected to a post-growth heat treatment which involves annealing in the presence of CdCl$_2$. The treatment results in significant increases in conversion efficiency ($\eta$) and all three solar cell parameters $V_{oc}$, $FF$, and $J_{sc}$.

In this work, several variations of the CdCl$_2$ treatment were used on more than 100 samples to investigate their effects on the solar cell parameters. A vapor CdCl$_2$ method was applied for the treatment with various source temperatures, substrate temperatures, and treatment times. The cells were characterized by dark and light J-V and spectral response (SR) measurements.
CHAPTER ONE

INTRODUCTION

Photovoltaic conversion of solar energy is one of the most promising ways of meeting the increasing energy demands of the future in a time when conventional sources of energy are being exhausted. Photovoltaic conversion has many advantages over conventional energy conversion. Electricity produced from photovoltaics has a far smaller impact on the environment than traditional methods. Conventional methods (e.g. burning coal, petroleum and other fossil fuels, and waste incineration plants) produce pollutants such as carbon dioxide, carbon monoxide, and others. These pollutants are responsible for the greenhouse effect and global warming [25]. Furthermore, fossil fuels and uranium (nuclear energy) are non-renewable resources. The only resource needed to power a solar cell is sunlight. Since the sunlight is clean, abundant and virtually limitless, solar cells are non-polluting and a renewable alternative to conventional energy sources. As solar cells have a useful life in excess of twenty years, they can be considered as long-life devices [22]. Capturing solar energy typically requires equipment with a relatively high initial cost. However, over the lifetime of the solar equipment, these systems can prove to be cost-competitive, as compared to conventional energy technologies. The key to successful solar energy installation is to use quality components that have long lifetimes and require minimal maintenance.
A solar cell relies on a quantum mechanical process known as the “photovoltaic (PV) effect”. The conversion efficiency and performance of a solar cell depend on its material properties, design and fabrication process. Potential semiconductor materials used in solar cells are single crystalline silicon (Si), amorphous Si and polycrystalline thin films. Among polycrystalline thin films, copper-indium-diselenide (CuInSe$_2$) and cadmium-telluride (CdTe) are the most popular. The CdTe thin film solar cell is the topic of this thesis.

The primary objective of this research is to study the effect of a vapor CdCl$_2$ treatment on CdS/CdTe solar cells. This study has been carried out in order to improve the understanding of thin film CdTe solar cells and to develop improved processing schemes.

1.1 Background

The development of the solar cell stems from the work of the French physicist Antoine – Cesar Becquerel in 1839. Becquerel discovered the photovoltaic effect while experimenting with a solid electrode in an electrolyte solution; he observed that voltage developed when light fell upon an electrode. About 50 years later, Charles Fritts constructed the first true solar cells using junctions formed by coating the semiconductor selenium with an ultra-thin, nearly transparent layer of gold. Fritts’ devices were very inefficient, transforming less than 1% of the absorbed light into electrical energy.
By 1927, another metal semiconductor-junction solar cell, which was made of copper and the semiconductor copper oxide, had been demonstrated. By the 1930s both the selenium cell and the copper oxide cell were being employed in light-sensitive devices, such as photometers for use in photography. These early solar cells, however, still had energy-conversion efficiencies of less than 1%. This impasse was finally overcome with the development of the Si solar cell by Rusell Ohl in 1941. In 1954, three other American researchers, namely G.L. Pearson, Daryl Chapin, and Calvin Fuller, demonstrated a silicon solar cell capable of a 6% energy-conversion efficiency when used in direct sunlight. By the late 1980s Si cells, as well as those made of gallium arsenide (GaAs), with efficiencies of more than 20% [26] had been fabricated.

Since 1990, amorphous Si and polycrystalline thin film solar cell efficiency have improved appreciably. The efficiency for amorphous Si has been reported 12% in the lab and 7% for commercial cells [44]. In 1992, the University of South Florida fabricated thin film SnO$_2$/CdS/CdTe cell of 15.8% efficiency [41]. In 2002, the NREL (National Renewable Energy Laboratory) CdTe team have modified the CdTe device structure and fabricated a Cd$_2$SnO$_4$/Zn$_2$SnO$_4$/CdS/CdTe thin-film solar cell of 16.4% efficiency [42]. The concentrator solar cell is a special Si device in which sunlight is concentrated on to the cell surface by means of lenses. Efficiencies up to 30% have been reported for a concentrator [44]. A multijunction cell mostly uses GaAs as one or all of its component cells. These solar cells have efficiencies of more than 35% under concentrated sunlight [45].
1.2 Solar Energy

Since the sun is the light source for solar cells, knowledge of the exact distribution of the energy content in sunlight is important in solar cell work as these cells respond differently to different wavelengths of light. Solar energy is the radiative energy output in the form of electromagnetic waves, which the sun continually emits into space. The radiation reaching earth is scattered and absorbed in the atmosphere and the intensity is dependent upon the angle of incidence. The power level of the solar spectrum in outer space, where there is no absorption of the radiation, is about 1300 W/m$^2$ [25]. This is termed as air-mass-zero (AM0) spectrum. AM1.5 spectrum is the most widely used terrestrial standard for evaluating solar cells. It is the solar spectral irradiance distribution incident at sea level from the sun at $45^\circ$ above the horizon. The total incident power for AM 1.5 is 844 W/m$^2$ [21]. The maximum radiation is in the wavelength range of 500 to 600 nm as shown in figure 1.1. It would therefore be desirable that the response of solar cells in this region is high [10].
1.3 Solar Cell Basic Structure

The most common form of a solar cell is based on the photovoltaic (PV) effect in which light falling on a two layer semiconductor device produces a photo-voltage or potential difference between the layers. This voltage is capable of driving a current through an external circuit and thereby producing useful work.

A solar cell is basically a p-n junction photo diode with a large light sensitive area. The device structure of a solar cell consists of three main elements as shown in figure 1.2.

1. a semiconductor which absorbs light and converts it into electron-hole pairs (discussed in section 2.2.1).
(2) semiconductor junction or p-n junction (discussed in section 2.1) which separates the photo-generated carriers (electrons and holes), and

(3) contacts on the front and back of the cell that allow the current to flow to the external circuit.

The electrical contact layer on the face of the cell where light enters is generally present in some grid pattern and is composed of a good conductor such as metal. The grid pattern does not cover the entire face of the cell since grid material, though good electrical conductors are generally not transparent to light. Hence, the grid pattern must be widely spaced to allow light to enter the solar cell but not to the extent that the electrical contact layer will have difficulty in collecting the current produced by the cell. The back electrical contact layer has no such diametrically opposed restrictions. Its function is simply as an electrical contact and thus covers the entire back surface of the cell structure. Because the back layer must be a very good electrical conductor, it is
always made of metal. For thin film solar cells like CdTe and CIGS front contact is transparent instead of grid. A transparent conducting oxide (TCO), the SnO$_2$ is commonly used as front contact which has a low electrical sheet resistance and high optical transmission.
CHAPTER TWO

THEORY

Understanding of the fundamental theory behind the design of solar cells is very important for fabricating high efficiency solar cells. The main part of a solar cell is the p-n junction and its functionality involves the photovoltaic effect. These terms are explained in the following sections.

2.1 p-n Junction

Figure 2.1 shows energy band diagram for n-type and p-type semiconductors before they form a junction. When n-and p-type semiconductors are brought in contact, free electrons move from n-type to p-type and holes from p-type to n-type. This movement of carriers occurs by diffusion and its direction is from higher concentration to lower [11]. As the diffusion process proceeds an electric field starts to induce due to the accumulation of static charges on both sides of the junction. A net negative charge on the p-side and positive charge on the n-side build up. This charged area is called the space charge region or depletion region. The diffusion process stops when the effect of
concentration gradient of carriers is balanced by the electric field at the junction region [25].

Figure 2.1 Band Structures of n-type and p-type Semiconductors of Same Material

At the junction the Fermi levels in both sides are forced to line up, causing the valance and conduction bands to bend as shown in figure 2.2. The difference in the potential energy of electrons at two sides of the junction is referred to as the built-in potential, $V_{bi}$. The electric field plays a very important role in the photovoltaic effect.

Figure 2.2 Homojunction Energy Band Diagram

A p-n junction can be a homojunction (both sides of the junction are made of same material) or a heterojunction (two sides of the junction are made of different
materials). Both of them have their own merits and demerits regarding the design issues of solar cells. A homojunction has perfect band alignment. The use of the same material results in perfect lattice match on either side of the junction. Lattice match helps to reduce interfacial traps, which can be responsible for reducing carrier lifetime by recombination when they exist in the vicinity of the junction.

On the other hand, a heterojunction may show a discontinuity in the band alignment, more prominent in the conduction band which may cause to form an abrupt metallurgical junction. The difference (discontinuity) in energy of the conduction band edges in the two semiconductors is represented by $\Delta E_c$ and that in the valence band edges by $\Delta E_v$ as shown in figure 2.3. The equations for the discontinuities are given by

$$\Delta E_c = (X_1-X_2)q \quad \text{…. (2.1)}$$
$$\Delta E_v = \Delta E_g - \Delta E_c \quad \text{…. (2.2)}$$

where $X_1$ and $X_2$ are the electron affinities for p and n type semiconductors respectively, $\Delta E_g$ is the band gap difference, $q$ is the electron charge ($q = 1.602 \times 10^{-19}$ Coulombs). The dimensions for $\Delta E_c$, $\Delta E_v$, $\Delta E_g$ are eV and for $X_1$, $X_2$ are volts. The $\Delta E_c$ and $\Delta E_v$ depend on the material properties of the p and n-type semiconductors.

If a careful material selection is not made, lattice mismatch and interface traps can be a problem for device performance. However many junctions are fabricated at high enough temperatures so that some interdiffusion occurs and reduces lattice mismatch. For a solar cell, the band gap and absorption coefficient of the absorber are very important. A heterojunction can help significantly in that issue. In a heterojunction like
the CdS/CdTe solar cell, the window layer (CdS) may have a wider band gap than the absorber (CdTe) as shown in figure 2.4. This wider band gap will allow greater current generation from high energy photons.

![Heterojunction Energy Band Diagram](image1)

**Figure 2.3** Heterojunction Energy Band Diagram

![Energy Band Diagram for the CdS/CdTe Solar Cell](image2)

**Figure 2.4** Energy Band Diagram for the CdS/CdTe Solar Cell
2.2 Photovoltaic Effect

The photovoltaic effect is the generation of an electromotive force as a result of the absorption of radiation. It can occur in gases, liquids, and solids, but it is in solids, especially in semiconductors, that acceptable efficiencies for conversion of solar energy into electric power have been observed [1].

The photovoltaic effect consists of the following four essential processes.

1. Absorption of radiation and generation of charge carriers (electron-hole pairs) in the semiconductors.
2. Separation of generated carrier pairs at the junction, a region of electrostatic field.
3. Migration of carriers to a junction
4. Collection of these carriers at the contacts of the device

2.2.1 Absorption of Radiation and Generation of Charge Carriers

When a beam of monochromatic radiation is incident on a homogeneous solid, the relation between the intensity $I(X)$ at a distance $X$ from the surface and the intensity on the surface $I(0)$ can be expressed as follows:

$$I(X) = I(0)e^{-\alpha X} \quad \ldots (2.3)$$

where $\alpha$ is the absorption coefficient, and $X$ is the distance measured along the axis normal to the plane of constant phase of the incident electromagnetic wave. The dimensions for $X$ is cm and for $\alpha$ is cm$^{-1}$. $\alpha$ is a function of the wavelength or photon
energy \((h \nu)\) of the incident radiation. It determines how far below the surface of the cell light of a given wavelength is absorbed. Figure 2.5 shows a plot of \(\ln \alpha vs (h \nu)\) for several semiconductors used in fabricating solar cells.

![Figure 2.5 Absorption Coefficient \((\alpha) vs Photon Energy \((h \nu)\) for Materials Used in Solar Cells](image)

Figure 2.5 Absorption Coefficient \((\alpha) vs Photon Energy \((h \nu)\) for Materials Used in Solar Cells
Curves shown in figure 2.5 are characterized by a threshold for absorption which corresponds to a photon energy equal to the energy band gap ($E_g$) of the semiconductor. For a photon with an energy $(h\nu) < E_g$, the values of $\alpha$ in general are very small while $\alpha$ rises for $(h\nu) > E_g$ to values of $10^4$ to $10^5$ cm$^{-1}$ [1]. Absorption of photons occurs when $(h\nu) \geq E_g$ and electron-hole pairs are generated as shown in figure 2.6. According to figure 2.5, there are basically two kinds of absorption curves, those for direct band gap semiconductors such as gallium arsenide (GaAs), CdS, CdTe etc. which rise very sharply near the band gap energy, and those for indirect band gap semiconductors like Si which increase gradually.

Since most of the incident solar energy will be absorbed in a few micrometers in direct gap semiconductors, they are suitable for the fabrication of thin film solar cells. CdTe has high absorption coefficient and a layer as thin as 2 μm can absorb most of the incident radiation. On the other hand, the indirect band gap semiconductors such as Si have low absorption coefficient and considerably thicker layers (more than 100 μm ) are required to absorb most of the incident radiation.
2.2.2 Separation of Carriers at Junction

Absorption of each photon results in the creation of a free electron and a free hole. In order to get a photogenerated current these free carrier pairs have to be separated before they recombine. The built-in field (in figure 2.7) is a very powerful separator of oppositely charged free carriers once they are within its influence. The electric field opposes electrons flowing from the n-type region to the p-type region but it favors electrons moving from the p-type region to the n-type region. If photo generated electrons encounter the electric field, they will be driven “downhill” across the interface to the other side. Similarly a light generated free hole formed (along with a free electron) on the n-type might be pushed by the built-in-field into the p-type lattice. Thus the light generated electrons would be sent one way by the field, and holes would be accelerated the other way as shown in figure 2.8. Under illumination, minority carriers carry the current and both electrons and holes contribute to the current flow.

Almost every electron-hole pair generated by light absorbed within the electric field region could be separated and contribute to the current. This would provide near perfect separation of electrons and holes. The field driven movement of free carriers within the built-in-field is called drift.
Figure 2.7  Built-in Electric Field in p-n Junction

Figure 2.8  Band Diagram Under Illumination Showing the Direction of Motion of Minority Carriers by Built-in Field
2.2.3 Migration of Carriers to a Junction

The free carrier pairs generated by the absorption of radiation outside of the field region must remain separated sufficiently long enough to travel to the charge separation site: the junction. Fortunately, electrons and holes freed by the absorption of light do not instantly lose their energy and fall back into bound states. The amount of time they remain mobile is called their lifetime.

If no recombination occurs, during the lifetime the carriers may encounter the built-in-field by diffusion and accelerate to the other side of the device. The minority carrier lifetime in intrinsic semiconductors depends on whether the semiconductor is a direct or indirect band gap material. In direct band gap materials, the lifetime is governed by direct band to band recombination and is short, less than $10^{-8}$ second in intrinsic material. Therefore it is hardly affected by the presence of recombination centers. In intrinsic silicon, crystals of good structural perfection, the minority carrier lifetime is on the order of several milliseconds. Hence, it is easily reduced by recombination centers, such as point defects, dislocations, and certain foreign atoms. Since the thickness of the material needed to absorb most of the solar radiation is smaller in direct than in indirect gap materials, the shorter lifetime in the direct gap materials is not necessarily a disadvantage to the fabrication of efficient solar cells [6].

Besides bulk recombination, some of the free carriers generated close to the surface layer of solar cells are lost by surface recombination without contributing to the generation of current. Since most of the solar radiation is absorbed close to the surface layer, it is very important to prepare the surface in such a way that free carriers lost due to
surface recombination can be minimized. In practice, it is impossible to eliminate completely the effects of surface states.

2.3 Solar Cell Device Physics

A solar cell is a large area diode with shallow junction depth to collect solar radiation effectively. The forward dark current relationship of a solar cell can be expressed as

$$J = J_o \left[ \exp \left( \frac{qV}{AkT} \right) - 1 \right]$$

.... (2.4)

where, $J$ is the external current flow, $J_o$ is the reverse saturation current, $q$ is the electronic charge ($q = 1.602 \times 10^{-19}$ Coulombs), $V$ is the applied voltage, $k$ is the Boltzmann constant which equals to $1.38 \times 10^{-23}$ J/K, $T$ is the absolute temperature and $A$ is the “ideality factor” of a diode, which depends on the dominating transport mechanism and usually varies from 1 to 2. $A$ equals 1 when the diffusion current dominates and $A$ equals 2 when the recombination current dominates. When both currents are comparable, $A$ has a value between 1 and 2. The dimensions for $J, J_o$ are amp/cm$^2$ and for $V$ is volt.

![The Equivalent Circuits of a Solar Cell Under Illumination](image)

Figure 2.9 The Equivalent Circuits of a Solar Cell Under Illumination
The model of a solar cell shown in figure 2.9 represents a diode in parallel with a light induced current source. $J_L$ is the magnitude of the photo generated current, and $R_s$, $R_{sh}$ represent the series and shunt resistance respectively. The dimension for $J_L$ is amp/cm$^2$ and for $R_s$, $R_{sh}$ are $\Omega\cdot$cm$^2$. $R_s$ is due to the bulk resistance of the semiconductor and the resistance of the contacts and interconnections. The losses due to leakage currents and lattice defects are represented by $R_{sh}$.

In ideal case, ($R_s = 0$, and $R_{sh} = \alpha$) the current through a device as depicted in above figure can be given by

$$J = J_o [(\exp \frac{qV}{AkT}) - 1] - J_L \quad \text{…. (2.5)}$$

In practical device series and shunt resistance affects the device performance and can no longer be neglected. Incorporating $R_s$ and $R_{sh}$

$$J = J_o [(\exp \frac{q(V - JR_s)}{AkT}) - 1] + \left[ \frac{V - JR_s}{R_{sh}} \right] - J_L \quad \text{…. (2.6)}$$

In this equation the carrier collection loss is ignored. However in real cells, especially non-lattice-matched heterojunctions, there is some collection loss. It is bias voltage dependant and decreases with forward bias, resulting in reduced fill factor (FF) and open circuit voltage ($V_{oc}$). When the bias voltage dependency of the collection is considered then $J_L$ would be replaced by $H(V) J_L$ [28]. Equation 2.4 becomes,

$$J = J_o [(\exp \frac{q(V - JR_s)}{AkT}) - 1] + \left[ \frac{V - JR_s}{R_{sh}} \right] - H(V) J_L \quad \text{…. (2.7)}$$
The factor \( H(V) \) is called collection function. For large reverse bias, \( H=1 \) and \( J \) follows the ideal curve. For \( H<1 \), the value of light generated current collected is reduced with respect to that generated in the absorber, especially for forward bias. As a result \( V_{oc} \) is reduced slightly and there is a considerable reduction in \( FF \). The reduction in short circuit current \( (J_{sc}) \) is usually quite small in efficient cells.

Figure 2.10 shows a current–voltage \( (J-V) \) curve of a typical solar cell measured both in the dark and under illumination. The \( J-V \) curve describes three important parameters that give complete description of the solar cell: \( J_{sc} \), \( V_{oc} \), and \( FF \).

\( J_{sc} \) is obtained when the external terminals of the cell are shorted. In this situation there can be no change in potential drop across the sample, since its terminals are shorted. The height of the internal barrier is thus the same as the equilibrium height, and the external voltage is zero. Under ideal conditions \( J_{sc} \) is \( J_L \). However, \( J_{sc} \) can be lower than \( J_L \) due to the effect of \( R_s \), \( R_{sh} \) or \( H(V) \).

When the external terminals are opened, there is no current flow in the external circuit. \( V_{oc} \) is obtained when \( J=0 \).

\[
V_{oc} = \frac{AkT}{q} \ln\left( \frac{J_L}{J_0} + 1 \right) \quad \ldots (2.8)
\]

The maximum output power, \( P_{max} \) is determined from the power rectangle, which is a rectangle with maximum area that can be fitted between the x and y-axis of the illuminated \( J-V \) curve.

\[
P_{max} = J_m \times V_m \quad \ldots (2.9)
\]
The ratio of the experimental power rectangle and theoretical rectangle is called the fill factor, $FF$.

$$FF = \frac{J_m V_m}{J_{sc} V_{oc}} \quad \ldots (2.10)$$

The conversion efficiency ($\eta$) of a solar cell is calculated in terms of power converted from electromagnetic radiation to electric power ($\text{Amperes} \times \text{Volts} = \text{Watts}$).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{FF V_{oc} J_{sc}}{P_{in}} \quad \ldots (2.11)$$

The normalized standard of $P_{in}$ is 100mW/cm$^2$. 

---

Figure 2.10 The Current-Voltage Curve of a p-n Junction Solar Cell (a) in the Dark and (b) Under Illumination
$J_{sc}$ can be obtained from the $J-V$ curve. A more accurate method for this is the spectral response (SR). SR for a device is obtained by plotting the quantum efficiency (Q.E.) as a function of radiation wavelength. Q.E. of a photon of wave length $\lambda$ is the probability that the photon contributes an electron to the photo current. It is the measure of the effectiveness of a device to produce electronic charge from the incident photon.

$$Q.E.(\lambda) = \frac{1}{q} \frac{hc}{\lambda} \frac{J_{sc}(\lambda)}{P(\lambda)} \hspace{1cm} \text{(2.12)}$$

where, $q$ is the unit charge, $\lambda$ is the photon wave length, $h$ is the Plank’s constant, $c$ is the speed of light in air, $J_{sc}(\lambda)$ is the short circuit current and $P(\lambda)$ is the incident light power.

2.4 Estimation of $R_s$, $R_{sh}$ and Identification of Back Barrier

A CdS/CdTe solar has a series resistance associated with it. In the simplest scenario this could be due to the resistivity of all three layers of SnO$_2$, CdS, and CdTe. It is assumed that $R_s$ is mostly due to CdTe resistivity.

$R_{sh}$ is considered when there is a shunt current due to several reasons such as thin CdS with voids and pinholes in it. Barrier can be formed at junctions due to difference in work functions of different materials. All these factors affect the J-V characteristics of the solar cells. Therefore determination of these is crucial.

$R_s$ and $R_{sh}$ can be estimated from the dV/dJ vs V graph shown in figure 2.11. The average value of dV/dJ at voltage range - 1.5 V to - 2.0 V is used as an estimation of $R_{sh}$. 

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in this thesis. An estimation of $R_s$ can be taken from $dV/dJ$ at high current and where $dV/dJ$ become constant (horizontal to X-axis). If $dV/dJ$ does not approach a constant value then the value of $dV/dJ$ represents an upper estimation.

The presence of a back barrier in the device can be determined if there is an inflection in $dV/dJ$. If dark $dV/dJ$ vs $V$ plot shows an inflection but the light $J-V$ does not, it is considered that the barrier is located at the front (near or at the CdS/CdTe junction). If the barrier remains under light then it is assumed to be at the back contact since no light can reach this region of the device. CdTe absorbs incoming light within 1 µ to 2 µ of thickness and the rest of CdTe thickness does not absorb any light. Therefore there is a possibility for the back barrier to remain there.

Figure 2.11 Estimation of $R_s$, $R_{sh}$, and Determination of Back Barrier
CHAPTER THREE

PROCESSING OF CdS/CdTe SOLAR CELLS

3.1.1 Device Fabrication

Fabrication of thin film CdS/CdTe solar cells involves a number of sequential processing steps to deposit various layers of the device structure. First of all fluorine doped SnO$_2$ (typically 10 $\Omega$/□) was deposited by metal organic chemical vapor deposition (MOCVD) on borosilicate glass substrates. The CdS films were deposited to a thickness of approximately 0.1 $\mu$m by the chemical bath deposition (CBD) technique, and CdTe was deposited by the close-spaced sublimation (CSS) process. The post deposition CdCl$_2$ heat treatment was accomplished by the vapor method. The devices were then masked and contacted with HgTe:Cu doped graphite paste. Finally the devices were given a back contact heat treatment at 270$^\circ$C for 25 min. Figure 3.1 shows the various layers of solar cells as per the sequence of device structure.
3.2 Properties of Different Layers of Cell Structure

The properties of the various components of the solar cells are explained in the followings sections.

3.2.1 Glass

The solar cell is produced on a substrate of 7059 Corning glass. The glass is transparent and allows light to pass through. Its thickness is 0.8 mm. It protects the active layers from the environment and provides mechanical strength.
3.2.2 SnO$_2$

Thin film fluorine doped tin-oxide (SnO$_2$:F) serves as the transparent conductive oxide (TCO) for the substrate. The function of the transparent conducting oxide coated glass substrate is to provide a highly transparent and conductive contact to the CdS window layer. SnO$_2$ has a large band gap of 3.2 eV. It has a low sheet resistance (10 $\Omega$/$\square$) and high optical transmission. SnO$_2$ is used as the front contact of a solar cell. Low sheet resistance of a contact on a semiconductor device is necessary to reduce the barrier to carrier flow between the semiconductor device and the external electronic circuit. High optical transmission is very important to increase the amount of electromagnetic radiation that is absorbed by the semiconductor material, thereby optimizing the operation of the photovoltaic device by maximizing the number of photo-generated electrons available for collection.

About 0.8 $\mu$m thick SnO$_2$ was deposited by MOCVD. During the MOCVD process, the SnO$_2$ is deposited at 450 - 550°C. It is very stable at high temperatures and inert ambient. However, it reacts with H$_2$ at the temperature above 390° C.

3.2.3 CdS

The polycrystalline n-CdS layer is an essential component of the cell as it contributes one half of the p-n junction. CdS should be conductive (n~10$^{16}$ cm$^{-3}$), thin to allow high transmission, and uniform to avoid shunt effects. Its band gap is 2.4 eV at
300K. Being a wide band gap material it is transparent to wavelengths of around 515 nm and above, and therefore it is referred to as the window layer. The thickness of the CdS layer is critical. Enhancing the photocurrent of CdTe solar cells by using thinner CdS films typically leads to lower $V_{oc}$ and $FF$. This is due to the presence of pinholes in CdS, which leads to the direct contact of the CdTe with TCO. For thicker CdS, absorption in CdS window layer below 510 nm can cause substantial current loss. It is experimentally found that 0.1 µm thickness of CdS provides the optimum cell performance. The CdS thickness reported here is the initial thickness and the final CdS thickness may vary considerably from the as deposited value due to partial consumption of the CdS films during the cell fabrication process. CdS was deposited by the CBD method.

3.2.4 CdTe

CdTe has long been recognized as a leading thin film photovoltaic material due to its near optimum band gap of 1.45 eV and high absorption coefficient. CdTe absorbs over 90% of available photons ($h\nu > 1.45$ eV) in less than 2 µm thickness. It is called the absorber layer. CdTe is polycrystalline and is p-type doped. The doping level of CdTe is less than that of CdS and the depletion region is mostly within the CdTe layer. This is therefore the active region of the solar cell, where most of the carrier generation and collection occurs. The grain size of CdTe increases with increasing substrate temperature. The basic requirements for efficient absorption and photo current generation are uniform CdTe film with thickness ~2 µm, low density of defects, larger
grain size (>0.5 μm), and free of pinholes and voids. For our samples, thicker layer of CdTe ( ~5 μm ) is used to ensure homogeneity. CdTe was deposited by CSS technique.

The CdS/CdTe is given a post deposition CdCl$_2$ heat treatment which enables grain enhancement, reduces the defect density in the films, promotes the interdiffusion of the CdTe and CdS layers and thereby improves solar cell efficiency.

In base line process, CdCl$_2$ treatment is done by evaporation which involves deposition of CdCl$_2$ by physical vapor deposition (PVD) process and it requires a subsequent annealing. Alternative to this process is Vapor CdCl$_2$ method. These processes are described in details in the main body of chapter four.

3.2.5 Back Contact

Formation of low resistance back contacts to p-CdTe is needed for the fabrication of high efficiency solar cells. CdTe has a high electron affinity ($\chi = 4.5$ eV) and no metal exists with a high work function ($\phi_m$); consequently a Schottky barrier height given by the expression $\phi_b = (\chi + E_g) - \phi_m$, where $\chi$ is the electron affinity and $E_g$ is the band gap of the semiconductor exists [4]. All contacts to p-CdTe therefore have a barrier which has the opposite sense to that of the p-n junction as shown in Figure 3.2. Given that a back contact barrier is inevitable, some consider that a barrier height of less than 200 meV will be acceptable for device operation [4].

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The back contact generally includes two layers: the primary layer is a heavily doped layer that makes a low-loss electrical contact to the CdTe; and the secondary contact is metal that carries the current laterally [3]. The primary layer employs Cu, because the Cu diffuses into the CdTe and produces a heavily doped p-layer. This helps to reduce barrier height between CdTe and back contact. The copper can be introduced by mixing HgTe:Cu into the graphite. The graphite pasted films are then annealed at 270°C for 25 minutes in vacuum.
3.3 Deposition Methods

The various deposition methods used for the fabrication of CdTe cells in this thesis are described in this section.

3.3.1 Chemical Vapor Deposition

In chemical vapor deposition technique (CVD), thin films are deposited on the surface of a hot substrate by thermal decomposition or reaction of gaseous compounds when precursor gases are flown to the reaction chamber with the help of a carrier gas. When a metal organic material is used as precursor, the method is called metal organic chemical vapor deposition (MOCVD). SnO$_2$ was deposited by this method in a reaction chamber. A temperature of about 450$^\circ$C (18.2 mV) was maintained by RF heating. The precursors were TMT (tetramethyl tin) and oxygen. Halocarbon 13B1 was used as a dopant during the deposition. Helium was used as carrier gas for TMT. The flow of the gases was controlled by a mass flow controller (MFC). The SnO$_2$ is deposited as bi-layer. One layer is doped SnO$_2$:F and the other is undoped SnO$_2$. The undoped layer is highly resistive and is called the buffered layer. The buffered layer is required to have a good $V_{oc}$ and $FF$.

The chemical reaction occurs as follows [43]:

$$\text{Sn(CH}_3\text{)}_4(\text{vap}) + 8 \text{O}_2(\text{gas}) \rightarrow \text{SnO}_2(\text{solid}) + 4 \text{CO}_2(\text{gas}) + 6 \text{H}_2\text{O}(\text{gas}).$$
3.3.2 Chemical Bath Deposition

The chemical bath deposition (CBD) is a wet chemical method based on a slow, controlled decomposition of Thiourea in alkaline solution and the presence of Cd\(^{2+}\) ions. This low temperature deposition technique uses a controlled chemical reaction to affect the deposition of a thin film by precipitation. CdS was deposited by this technique. The precursors for Cadmium and Sulfur were aqueous Cadmium acetate (Cd(CH\(_3\)COO)\(_2\)) and Thiourea ((NH\(_2\))\(_2\)CS) respectively. Certain proportion of Cadmium acetate, Ammonium hydroxide (a base), Ammonium acetate (buffer solution), and H\(_2\)O were mixed to make a solution. A measured volume of prepared solution and Thiourea were added at a specific time intervals to 600 ml of H\(_2\)O in a double jacketed beaker. The bath was maintained at a constant temperature of 85\(^{\circ}\)C by circulating ethylene glycol through the hollow walls of the beaker.

The reaction proceeds in aqueous solution as follows [40]:

\[
\text{Cd(CH}_3\text{COO)}_2 + (\text{NH}_2)_2\text{C= S} + 2\text{OH}^- \rightarrow \text{CdS}^{(s)} + \text{H}_2\text{CN}_2 + 2\text{H}_2\text{O} + 2 \text{CH}_3\text{COO}^-
\]

3.3.3 Close Spaced Sublimation

The CdTe films were deposited by close spaced sublimation (CSS) to a thickness of approximately 5\(\mu\)m. CdTe chunks were first sublimed in a source plate. The substrate is placed at a spacing of several millimeters from the source. The source and the substrate are heated by 2000W halogen lamps. From the source, CdTe is deposited to the
substrate. Source and substrate temperatures were 680°C and 580°C respectively. Deposition rate is ~1 µm/min. The temperature of substrate holder is less than that of the source to allow for condensation of the CdTe. The deposition of CdTe films by CSS technique is based on the reversible dissociation of the CdTe at high temperatures as follows [27]:

\[ \text{CdTe (s)} \leftrightarrow \text{Cd (g)} + \text{Te (g)} \]

3.3.4 Physical Vapor Deposition

Physical vapor deposition (PVD) is similar to CVD. In both cases Vapor is being deposited on to the substrate. What is different between PVD and CVD is how the material is transported in vapor form to the substrate where it is deposited. In PVD, the particles to be deposited are carried by a physical means to the substrate where in CVD, the particles are carried through a chemical reaction. The precursor for the PVD is a solid. At high vacuum conditions the solid is first converted to liquid and then to vapor. Because of the high vacuum conditions the vapor is deposited directly on the substrate. This is what is used as baseline process for CdCl\(_2\) treatment. The description of this method is given in details in chapter four.
3.3.5 Graphite Paste Application

After CdCl$_2$ treatment, the samples are prepared for back contacting. The back contacts consisted of a HgTe-doped graphite paste (10 gm graphite: 4 gm HgTe:Cu) and a silver ($\text{Ag}$) electrode. Before graphite paste application, the evaporated CdCl$_2$ treated samples are etched in a bromine/methanol solution for 8 seconds and blown to dry. This helps to make a Te rich surface [39]. Immediately afterwards, the samples were masked for the front contact and the graphite paste was applied to the samples with a spatula.

Back contact annealing was performed in He gas ambient at 270°F for 25 minutes. The graphite was then planarized, and subsequently the silver was applied using a brush.

Finally, the mask was removed and the front contact patterns were scribed on the SnO$_2$. Indium was put on top of the SnO$_2$ with the help of a soldering iron to make the front contact more conductive.

3.4 Solar Cell Measurements

A specific LabView program was used to collect the J-V data. A Keithley 2410 1100 V Source Meter supplied the power. A generic solar simulator was utilized for light J-V. The solar simulator was calibrated at 100 mW/cm$^2$. The voltage and current values were read by the same instrument. The $V_{oc}$ and $FF$ along with the J-V plots were calculated and displayed on the monitor.
For spectral response measurements, an Oriel Cornerstone monochromator (model 74100) was used. The light source was a GE 400W/120V Quartz Line lamp (model # 43707). A Lab View program operated the spectral response setup. The short circuit current was obtained from the quantum efficiency plots.
CHAPTER FOUR

CdCl₂ TREATMENT

The CdCl₂ heat treatment is a key processing step in the fabrication of thin film CdTe solar cells. After decades of research it has been confirmed that it increases the solar cell efficiency significantly. But still there are many queries in various aspects of the CdCl₂ treatment that keep many researchers involved to explore the effects of CdCl₂ in solar cell processing.

4.1 Process Flow Diagram

CdCl₂ treatment is applied after deposition of the CdTe absorber layer and prior to the application of the back contact. Figure 4.1 shows the process flow diagram.

From figure 4.1 it can be seen that the vapor CdCl₂ treatment involves less processing steps than evaporated CdCl₂ treatment. The vapor treatment is a single step process to have a reaction among O₂, Te, Cd, and Cl. The evaporated method is a two step process in which CdCl₂ deposition and annealing need to be performed sequentially.
in two different chambers. Again, evaporated treatment involves an extra step for etching prior to back contact which vapor treatment does not.

**Figure 4.1 Process Flow Diagram**

4.2 **CdCl$_2$ Treatment Methods**

Commonly used methods for CdCl$_2$ treatment are:

1. Solution CdCl$_2$ treatment
2. Evaporated CdCl$_2$ treatment
3. Vapor CdCl$_2$ treatment

This work was limited to evaporated CdCl$_2$ and vapor CdCl$_2$ treatment.
4.2.1 Solution CdCl$_2$ Treatment

It is the most common and simple process which involves soaking the CdTe films in the methanol containing dissolved CdCl$_2$ and then heating [7]. Although this technique has been very popular and easy to carry out for laboratory size solar cells, it is not as attractive for manufacturing process, since it involves the use of Cd containing solutions. Another shortcoming of this technique is the fact that significant CdCl$_2$ residue remains on the CdTe surface and must be removed after the treatment is completed, adding more processing steps to the overall process.

4.2.2 Evaporated CdCl$_2$ Treatment

A variation of the wet process involves evaporation of CdCl$_2$ on CdTe eliminates the use of solutions. In evaporated CdCl$_2$ treatment 99.99% pure CdCl$_2$ pellets (source) were placed in a stainless steel case. The top cover of the case was porous to allow a regulated flow of CdCl$_2$ vapor to the substrate. Substrates were placed approximately 15 cm above the source boat. They were supported by a stainless steel frame mounted upon a quartz tube through which the evaporation took place. Deposition took place in a high vacuum chamber. The substrates were not heated during the process and the CdCl$_2$ films were deposited normally to a thickness of 8000 Å. CdCl$_2$ thickness was obtained from a thickness monitor. The evaporation chamber used for this work is shown in figure 4.2.
Following deposition, the samples were annealed in He/O$_2$ ambient normally at 390°C for 25 min.
4.2.3 Vapor CdCl$_2$ Method

The vapor treatment eliminates processing steps that are needed for the evaporation-based treatment. In vapor treatment, the samples are exposed to CdCl$_2$ vapors during the heat treatment. Therefore a complete treatment is done at the same chamber. In addition etching in the CdTe sample for the back contact can be eliminated [24].

The vapor treatment was carried out in a 2-zone tube furnace, where 99.99% anhydrous CdCl$_2$ pellets were placed in a graphite crucible at one zone and the CdTe cell on a graphite plate at the other. The temperature of each zone was controlled independently using quartz lamps for heating. The furnace was kept at atmospheric pressure and the CdCl$_2$ vapors were transported to the sample zone using a carrier gas. The carrier gas was a mixture of He and O$_2$. Initially the furnace was purged with He for 10 minutes. He and O$_2$ were passed though the furnace for 20 minutes prior to the start of the heat treatment. The annealing time varied from 15 seconds to 3 minutes. The annealing time is the time interval from the instant that the cells reached the predetermined annealing temperature until the heaters were turned off. Source/substrate temperatures, heat treatment times, and ambient were varied to find their effects on the samples.
4.2.3.1 Large Area Vapor CdCl$_2$ Chamber

A large area vapor chamber (3cm x 15 cm reactor) has been introduced in order to develop a batch process. It is basically the extension of the small area chamber described elsewhere [24]. The substrate holder is 3 cm x 15 cm graphite plate which is capable of supporting 4 substrates. The source and substrate holder are kept apart 3 cm by a quartz plate. The tube furnace employs 1 pair of halogen lamps for the source zone and 3 pairs for the substrate zone. The power of each lamp is 2000 watt. A schematic diagram of large area vapor CdCl$_2$ chamber is shown in figure 4.3 and a top view diagram of large area substrate holder in figure 4.4.

Figure 4.3 Large Area Vapor CdCl$_2$ Chamber
4.3 Role of $O_2$ in CdCl$_2$ Treatment

The presence of $O_2$ has been found to lead to consumption of the CdS films. It is possible that the $O_2$ annealed samples exhibit an improved interface as a result of enhanced interdiffusion between CdTe and CdS. It has also been found that controlling the $O_2$ concentration during the CdCl$_2$ treatment, the CdS consumption can be controlled and varied [29]. Deep level transient spectroscopy (DLTS) results have been found to be similar for both $O_2$ and He ambient. This suggests that the presence of $O_2$ does not affect the electronic defects in CdTe solar cells [8]. Again the amount of $O_2$ during the CdCl$_2$ treatment is important in determining the CdS consumption and, therefore, can affect the junction properties.
4.4 Effect of CdCl₂ Treatment

Various effects of CdCl₂ treatment are explained below.

4.4.1 Interdiffusion in CdS/CdTe Interface

In principle, one can not fabricate a good CdS/CdTe hetero-junction because of the great lattice mismatch between the two semiconductors as shown in figure 4.5. Lattice mismatch can occur in hetero-junctions as well as in polycrystalline grain boundaries. It becomes more critical for the cell performance when they are in hetero-junctions rather than in grain boundaries. Because the carriers generated in the semiconductors pass through the junction before they are collected at the device contacts. The CdCl₂ treatment helps to build an interfacial layer at the junction and reduces lattice mismatch.
The CdCl$_2$ heat treatment improves the CdS/CdTe junction by enhancing the inter-diffusion between the semiconductors leading to the formation of an alloyed CdTe$_x$S$_{1-x}$/CdS$_y$Te$_{1-y}$ interface, where x and y are less than or equal to the solubility limits at about 400 °C (x~0.03 and y~0.06) as shown in figure 4.6 [3].
This inter-diffusion process is considered to result in S-rich spikes along the grain boundaries. This S-rich material is likely to be n-type and could lead to enhance electron collection from the CdTe.

The effect of inter diffusion of CdTe into CdS is to curtail the spectral response at its low wavelength ($\lambda$) end by reducing the window transmission. On the other hand, incorporation of some CdS into the CdTe extends the spectral response to longer wave lengths [13]. The QE of figure 4.7 shows evidence of the S-Te interdiffusion. The reduced QE between 520 and 580 nm provides clear evidence of interdiffusion of Te into the CdS, (the band gap shrinks at a rate of about 2.7 eV per unit y with increasing Te content in the CdTe$_y$S$_{1-y}$). When cells are fabricated with no CdS layer, the red edge of the QE lies at about 855 nm, the band edge of pure CdTe, But when cells are fabricated with some CdS, part of the CdS layer is consumed and the QE extends an additional 10 to 20 nm into the near infrared—in some cases up to 885 nm. This is consistent with S diffusion into CdTe [3].

Figure 4.7  QE With and Without CdS Layers
The interface layer reduces the interface states density at the CdS/CdTe junction and recombination velocity. It is suspected that the inter-diffusion may be responsible for important electrical changes undergone by the cell during CdCl$_2$ processing. For example, inter-diffusion is associated with a decrease in the diode ideality factor, indicating a reduction in the interface state density [13].

4.4.2 Structural Properties - Recrystallization

From X-ray diffraction measurements for CdCl$_2$ vapor treated CdTe films, it has been found that the lattice constant increases from 6.437 to 6.479 Å, respectively, for CdCl$_2$ concentration from 1 to 5 wt. % (the amount of CdCl$_2$ in CdTe pellets). For 5 wt. % CdCl$_2$, the value of the lattice constant 'a' is near to that for a powder sample (6.481 Å) [30]. The reduction in the lattice constant value can be due to tensile stress in these films. The shift in the value of 'a' towards the powder sample value with increasing CdCl$_2$ concentration indicates that CdCl$_2$ reduces the stress in the CdTe films [14].

Figure 4.8 shows that most of CdTe X-ray diffraction peaks are present for films without CdCl$_2$ treatment. However, when CdCl$_2$ concentration increases to greater than 1.5 wt. %, the x-ray reflection is predominantly from the (111) plane and the reflections from all other planes become negligibly small. This indicates that in the presence of sufficient CdCl$_2$ vapor pressure, CdTe grains grow preferentially with (111) orientation. The dependence of CdCl$_2$ concentration indicates that CdCl$_2$ vapors somehow facilitating this oriented growth. This may be due to the increase in the mobility of Cd and Te$_2$ atoms.
in presence of CdCl₂. It is known that CdCl₂ acts as a catalyst in the CdTe film growth and it increases the atomic mobility of Cd and Te [14].

![Diffraction Spectra of CdCl₂ Treated CdTe Films](image)

Figure 4.8  Diffraction Spectra of CdCl₂ Treated CdTe Films

A similar behavior is observed in CdS. X-ray analysis for CdS films has shown that a single line at 26.65°, depicted in Figure 4.9 (a) is present before the treatment, which can be attributed to the [002] hexagonal phase as well as to the [111] cubic phase. On the contrary, after treatment, the hexagonal phase is more evident since, as is shown in Figure 4.9 (b), the [103] line clearly appears while the [002] line is narrowed indicating a better overall morphology [18].
Figure 4.9  X-ray Spectrum of CdS Layer (a) Before CdCl$_2$ Treatment, (b) After CdCl$_2$ Treatment
4.4.3 Morphology of the Films – Grain Enhancement

The CdCl$_2$ heat treatment is known to be beneficial in improving the performance of CdTe solar cells for various reasons. Among the improvements observed as a result of the CdCl$_2$ heat treatment is an increase in grain size typically observed in films with submicron size grains. Larger grain films (on the order of 1 µm or larger) do not undergo a grain enhancement, rather elimination of smaller grains present in such films has been observed [31]. SEM (Scanning Electron Microscope) measurements were carried out to determine the surface morphology of the films. Figure 4.10 shows the impact of CdCl$_2$ on the morphology in the CdTe films. The grain size increases drastically with CdCl$_2$ concentration. Grain size has been increased from 0.1 to >1 µm for a 5 wt.% CdCl$_2$ films [14].

![Figure 4.10 SEM Micrographs for CdTe Films](a) Before, and (b) After CdCl$_2$ Treatment
Figure 4.11 shows the AFM (atomic force microscopy) results for CdCl$_2$ treated CdS layer. CdS morphology remains good both before and after the treatment.

Figure 4.11  AFM Picture of CdS Layer (a) Before, and (b) After CdCl$_2$ Treatment [18]
Fourier transform analysis has indicated that the average lateral size of the crystallites has changed from 500 Å, before the treatment, to 2000 Å, after the treatment [18]. At higher CdCl₂ concentration the reduction of \( V_{oc} \) has been observed. A detailed analysis of the above results reveals that there can be two possible reasons for the reduction of \( V_{oc} \). The increase in CdCl₂ can lead to CdTe films grow with a degree of (111) preferred orientation and also help to grow large size grains. These growth conditions at higher CdCl₂ concentration not only promote the larger grain growth but also generate larger voids or pinholes between the grains. In addition to that, the reduction in the CdS thickness at higher CdCl₂ concentration exposes any flaws in the CdS films. All these lead to generation of micro-shunting paths in the CdS/CdTe junction and result in poor \( V_{oc} \) and \( FF \).

4.4.4 Type Conversion

As-deposited CdS is naturally n-type. However as-deposited CdTe is typically n-type and requires annealing in air or in the presence of a flux (i.e. CdCl₂) to cause type conversion and p-n junction formation. Therefore the process is often referred to an ‘activation’ or ‘type conversion’ process. It is stated that chlorine out diffusion combined with the slow cooling thermal treatment under tellurium pressure enables one to get high stable p-conductivity in CdTe layers recrystallized with CdCl₂ [23]. CdCl₂ is used both as a source of dopant in the CdS layer as a general sintering flux to modify the crystal size and orientation of the CdS and CdTe layers and improves the layers’ structure and
conductivity. The low resistivity p-CdTe is indispensable for fabricating high efficiency solar cells. A resistivity as low as 100 Ω-cm has been reported [35], while untreated CdTe films exhibits a resistivity of $10^7$ Ω-cm.

The properties of CdTe greatly depend upon the concentration of the various electrically active defects. Substitutional chlorine is the donor in CdTe [32]. Interstitial chlorine is found to be an acceptor [33]. Chlorine also forms complexes with native defects in CdTe. A complex $V_{Cd}\cdot D$, where D would be Cl, has been proposed by some investigators [34, 35].

The diffusion coefficient of Cl in CdTe is low. So it is possible to get balance between substitutional chlorine and native defect concentrations in CdTe and to bound almost all chlorine to the shallow acceptor complexes such as $(V_{Cd}^{2-} - Cl_{Te}^+)^\cdot$. Another similar shallow acceptor complex in CdTe would be $(Te_i^{2-} - Cl_{Te}^+)^\cdot$. It is known that the chemical bond between chlorine and Te is strong, the chemical bond between chlorine and S is weak. So it is likely that under Te pressure, part of Te$_i$ would be bound near Cl$_{Te}$ forming the acceptor complex $(Te^{2-} - Cl_{Te}^+)^\cdot$.

Shallow acceptor Complex $(V_{Cd}^{2-} - Cl_{Te}^+)^\cdot$ or $(Te_i^{2-} - Cl_{Te}^+)^\cdot$ are believed to be responsible for the high p-type conductivity in CdTe layers formed with CdCl$_2$ flux [23].
4.4.5 Current Transport Mechanism

It is considered that the CdCl$_2$ treatment effects the conversion of CdTe from n- to p- type, lowers series resistance and is accompanied by a change in current transport mechanism from tunneling/interface recombination to recombination in the depletion region [13]. Current transport studies, that is temperature dependent I-V analysis of cells, before and after CdCl$_2$ treatment indicate a change in the current transport mechanism. CdCl$_2$ treatment improves the microstructure of the CdTe films and eliminates active states at the CdS/CdTe interface, presumably by interdiffusion [36], thereby changing the current transport mechanism. The electron transport mechanism is dominated by recombination at the CdS/CdTe interface prior to the CdCl$_2$ treatment and by depletion-region recombination after the treatment [37]. This suggests a decrease in the density of interfacial states. Some authors ascribe the effect at least partly to the reduction in the volume fraction of material influenced by grain boundaries due to grain growth.

In DLTS study of CSS CdTe/CdS cells with CdCl$_2$ treatment, a stable hole trap was observed in samples but its activation energy decrease smoothly (from 484±4 to 195±7 meV) with the increasing severity of the CdCl$_2$ treatment. This was accompanied by a decrease in capture cross section from 2.6x10$^{-13}$ to 3.5x10$^{-18}$ cm$^{-2}$. The change in the activation energy was due to the band gap change which is the effect of interdiffusion (about 40meV) [38]. The change is directly associated with band bending at the CdTe grain boundaries, i.e. the valance band deformation is decrease by CdCl$_2$ treatment.
4.4.6 Solar Cell Performance

The CdCl$_2$ treatment improves the structural, morphological and electrical properties of the CdTe solar cells which eventually results in a significant increase in solar cell conversion efficiency ($\eta$) and all three solar cell parameters $V_{oc}$, $J_{sc}$, and $FF$. Table 4.1 shows the improvement of solar cell parameters [36].

Table 4.1 Parameters of CdTe/CdS Cells in the As-deposited, Annealed (400°C for 30 Minutes in Air) and CdCl$_2$ Treated States

<table>
<thead>
<tr>
<th>processing</th>
<th>$V_{oc}$ (mV)</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>FF (%)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposited</td>
<td>0.55</td>
<td>6</td>
<td>39</td>
<td>1.6</td>
</tr>
<tr>
<td>Air annealed</td>
<td>0.55</td>
<td>15</td>
<td>39</td>
<td>3.6</td>
</tr>
<tr>
<td>CdCl$_2$ treated</td>
<td>0.68</td>
<td>26.7</td>
<td>56.7</td>
<td>10</td>
</tr>
</tbody>
</table>

It can be observed from table 4.1 that the air annealed samples are not improved much than the as-deposited samples. Only a significant increase in $J_{sc}$ is noticeable. Whereas all three solar cell parameters and the efficiency are increased at a great extent when they are CdCl$_2$ treated.
4.5 Summary

From the above discussions it can be concluded that the CdCl\textsubscript{2} treatment has a great influence in CdTe/CdS solar cells. It affects the CdTe cells in terms of the following properties.

1. interdiffusion at the CdS/CdTe interface
2. recrystallization
3. grain enhancement
4. CdTe defect levels
5. type conversion
6. current transport and
7. solar cell performance.
CHAPTER FIVE

RESULTS AND ANALYSIS

Test results and analysis are described in this chapter. All samples have been characterized by dark and light J-V and SR measurements. Various process parameters have been studied with respect to average $V_{oc}$ and $FF$ in the following sections.

5.1 Introduction

The objective of this work was to increase the reactor size in order to investigate potential uniformity issues. The initial size of the reactor was 3 x 3 cm$^2$ and the new size is 3 x 15 cm$^2$. Initial experiments showed non-uniform performance as shown in figure 5.1. After studying the temperature profile of the substrate heater it was found to be non-uniform (as shown in figure 5.2). The heaters were rearranged and a more uniform temperature profile was obtained as shown in figure 5.2. The rest of the experiments are carried out under this profile. Sample positions along the heater are always noted.
Figure 5.1  Performance Variation Before and After Recalibration

Figure 5.2  Substrate Heater Temperature Profile (1) Before (2) After Recalibration
Figure 5.1 and 5.2 show before and after recalibrations of temperature profiles and performance. From these it can be seen that the temperature is a critical parameter that must be carefully controlled.

The average $V_{oc}$ of four cells has been taken for each substrate at four different positions of the substrate holder. Various processing conditions have been studied. Table 5.1 shows average $V_{oc}$s for the various conditions at four different positions (1, 2, 3 and 4) of the substrate heater. Substrate positions 1, 2, 3, and 4 are located on the holder at 0.5 cm, 3.7 cm, 7.0 cm and 10 cm away from the front edge respectively. The average $V_{oc}$ at four different positions is also shown graphically in figure 5.3.

<table>
<thead>
<tr>
<th>Position</th>
<th>$V_{oc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>#2460/450C, 90s, 90 min CBD</td>
</tr>
<tr>
<td>1</td>
<td>785</td>
</tr>
<tr>
<td>2</td>
<td>770</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>760</td>
</tr>
</tbody>
</table>
Factors affecting the average $V_{oc}$ are described in the following sections.

5.2 Substrate Position

In general, there is a tendency for the average $V_{oc}$ to decrease toward the rear end of the substrate holder which is obvious in figure 5.3. A closer examination of the data indicates that the average $V_{oc}$ decreases with respect to the position away from the front edge of the holder for samples #3, #11, #28, and #29 all of which were heat treated with the source temperature of 460°C, while relatively constant average $V_{oc}$ values have been
observed for samples #6, #31 and #34 which were treated at a higher source temperature of 480°C as shown in figures 5.4 and 5.5.

Figure 5.4 Average $V_{oc}$ at Different Positions (460°C)

Figure 5.5 Average $V_{oc}$ at Different Positions (480°C)
Since the vapor pressure of CdCl$_2$ increases with temperature, the observed uniformity of average $V_{oc}$ at 480°C could be due to the availability of sufficient CdCl$_2$ vapor throughout the holder up to the rear edge.

5.2.1 J-V and SR for Largest Non-uniformity in Performance

In this section cells from run #28 that exhibit the largest performance variations are compared to determine the reasons for the non-uniformity. J-V and SR curves are shown in figure 5.6 and 5.7.
Figure 5.6  Dark J-V (top),  Light J-V (bottom) for Sample #28
Figure 5.7  SR Curves for #28

Table 5.2 shows the best device results for each position and table 5.3 shows $R_s$, $R_{sh}$ for the same devices.

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>Position</th>
<th>Max. $V_{oc}$ (mV)</th>
<th>FF (%)</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>Efficiency $\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#28 (1-8-B1-1a)</td>
<td>1</td>
<td>790</td>
<td>55</td>
<td>22.52</td>
<td>9.78</td>
</tr>
<tr>
<td>#28 (1-8-B1-2a)</td>
<td>2</td>
<td>770</td>
<td>46.4</td>
<td>22.17</td>
<td>7.92</td>
</tr>
<tr>
<td>#28 (1-8-B2-1d)</td>
<td>3</td>
<td>730</td>
<td>54.6</td>
<td>23.23</td>
<td>9.17</td>
</tr>
<tr>
<td>#28 (1-8-B2-2d)</td>
<td>4</td>
<td>710</td>
<td>51.6</td>
<td>21.39</td>
<td>7.83</td>
</tr>
</tbody>
</table>
Figure 5.6 shows the dark ln J-V (top-left). From this plot it can be seen that at low current, cells at positions 1, 2, 3 have very similar dark \( J \), while the cell at position 4 has a higher dark \( J \). That suggests that recombination in cell at position 4 is higher. The \( \text{CdCl}_2 \) vapor affects the defect levels in the CdTe and reduces recombination. \( \text{CdCl}_2 \) may have less effect on the cell at position 4 due to insufficient \( \text{CdCl}_2 \) vapor (\( \text{CdCl}_2 \) vapors are suspected to get depleted at this position as mentioned earlier). Therefore lack of \( \text{CdCl}_2 \) may be the cause for high recombination in cell 4.

Table 5.3  Series and Shunt Resistances for Run #28.

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>Device position</th>
<th>( R_{sh} ) (( \Omega )-cm(^2))</th>
<th>Dark ( R_s ) (( \Omega )-cm(^2))</th>
<th>Light ( R_s ) (( \Omega )-cm(^2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>#28 (1-8-B1-1a)</td>
<td>1</td>
<td>924</td>
<td>2.98</td>
<td>2.6</td>
</tr>
<tr>
<td>#28 (1-8-B1-2a)</td>
<td>2</td>
<td>920</td>
<td>3.42</td>
<td>5.27</td>
</tr>
<tr>
<td>#28 (1-8-B2-1d)</td>
<td>3</td>
<td>720</td>
<td>2.6</td>
<td>2.3</td>
</tr>
<tr>
<td>#28 (1-8-B2-2d)</td>
<td>4</td>
<td>800</td>
<td>1.8</td>
<td>2.0</td>
</tr>
</tbody>
</table>

From the linear dark J-V (figure 5.6 (top right)) at high current, the cells at positions 1 and 2, have lower dark \( J \) than that of cells 3 and 4. The reason is cell 1 and 2 have higher \( R_s \) in the dark as shown in table 5.3. From the light J-V (figure 5.6 (bottom-right)) at higher forward bias, cells 1 and 2 also show higher \( R_s \). \( R_s \) is the highest for cell #2 due to barrier which can be seen in the light dV/dJ curve (shown in figure A.1 of appendix A). Therefore the lowest \( FF \) of this device seems to be due to highest \( R_s \) which
is the effect of the back contact, and not the CdCl$_2$. From the light J-V (figure 5.6 (bottom-left)), $R_{sh}$ is similar for all four cells (700-900 $\Omega$-cm$^2$).

Figure 5.7 shows the SR of the four cells. # 4 shows collection related loss. From the blue region it can be seen that # 3 and #4 have thinner CdS which leads to low $V_{oc}$ for these devices. #1and #2 are different substrates from #3 and #4. Therefore there is a possibility for the variations of $V_{oc}$ to be due to the CdS thickness variation. However the trend from high to low $V_{oc}$ from cell positions 1 to 4 is still present.

Finally it can be concluded that the low FF of the devices is due to the back contact (more obvious in # 2) and low $J_{sc}$ of #4 is related to the CdCl$_2$. Gradual variations in $V_{oc}$ can be due to Cds thickness variation as well as the CdCl$_2$ effect.

5.3 Source Temperature

Two source temperatures of $460^\circ$C and $480^\circ$C have been applied to the samples in order to see the variation of average $V_{oc}$ and FF. The best average $V_{oc}$ has been found to be at position 1 for all the test samples as shown in figure 5.3. Further analysis on the effect of source temperature has been carried out based on the best average $V_{oc}$ and FF in this section.

Samples #2, #3, #11, #28, #29, and #41 have been tested at source temperature $460^\circ$C while samples #6, #7, #8, #12, #31, and #34 have been tested at $480^\circ$C. The effect of source temperature on average $V_{oc}$ and FF has been studied by keeping all the other
test conditions such as substrate temperature, treatment time and CBD time constant. Set 1 (sample #11 and #12) and Set 2 (sample #31 and #41) of similar conditions have been analyzed for varying source temperature as given in Table 5.4 and are plotted in figure 5.8. At lower substrate temperature (420°C), average $V_{oc}$ increases with increasing source temperature while at higher substrate temperature (430°C), average $V_{oc}$ shows the opposite trend as shown in figure 5.8. A similar trend has been found for FF.

Table 5.4  Samples of Same Conditions with Different Source Temperatures

<table>
<thead>
<tr>
<th></th>
<th>Set 1</th>
<th></th>
<th>Set 2</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample No.</td>
<td>#12</td>
<td>#11</td>
<td>#31</td>
<td>#41</td>
</tr>
<tr>
<td>Treatment time (s)</td>
<td>90</td>
<td>90</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>Source temp (°C)</td>
<td>480</td>
<td>460</td>
<td>480</td>
<td>460</td>
</tr>
<tr>
<td>Substrate temp (°C)</td>
<td>420</td>
<td>420</td>
<td>430</td>
<td>430</td>
</tr>
<tr>
<td>CBD time (min)</td>
<td>90</td>
<td>90</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>Max. Avg. $V_{oc}$ (mV)</td>
<td>827.5</td>
<td>815</td>
<td>770</td>
<td>787.5</td>
</tr>
<tr>
<td>FF (%)</td>
<td>65</td>
<td>61.8</td>
<td>59.6</td>
<td>60</td>
</tr>
</tbody>
</table>

The maximum average $V_{oc}$ of 828 mV and $FF$ of 65% have been obtained from sample #12 at 480°C source temperature.
5.3.1 J-V and SR Analysis

J-V and SR data are shown in figure 5.9 and 5.10 respectively. Table 5.5 shows the best device results for different source temperatures and table 5.6 shows $R_s$ and $R_{sh}$ for the same devices.
Figure 5.9  Dark (top) and Light (bottom) J-V for Samples #11 & #12 Annealed at Different Source Temperatures: 480 and 460°C
Figure 5.10  SR Curves for Source Temperatures of 480 and 460°C

Table 5.5  Cell Results for Samples #11 and #12(TSUB=420°C, t = 90 Seconds)

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>Source Temp(°C)</th>
<th>MaxV(oc) (mV)</th>
<th>FF (%)</th>
<th>Jsc (mA/cm²)</th>
<th>Efficiency η(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#11 (4-17-A12-1c)</td>
<td>460</td>
<td>830</td>
<td>67.1</td>
<td>22.81</td>
<td>12.70</td>
</tr>
<tr>
<td>#12 (4-17-A5-1b)</td>
<td>480</td>
<td>830</td>
<td>65</td>
<td>23.53</td>
<td>12.69</td>
</tr>
</tbody>
</table>
Table 5.6 $R_s$ and $R_{sh}$ for Samples of Various Source Temperatures

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Source Temp(ºC)</th>
<th>$R_{sh}$ (Ω-cm²)</th>
<th>Dark $R_s$ (Ω-cm²) (upper limit)</th>
<th>Light $R_s$(Ω-cm²) (upper limit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#11 (4-17-A12-1c)</td>
<td>460</td>
<td>1000</td>
<td>7</td>
<td>0.8</td>
</tr>
<tr>
<td>#12 (4-17-A5-1b)</td>
<td>480</td>
<td>1000</td>
<td>0.8</td>
<td>0.4</td>
</tr>
</tbody>
</table>

The dark ln J-V in figure 5.9 (top-left) show very similar dark currents for both devices. In the linear dark J-V (figure 5.9 (top-right)), the cell of 460 ºC shows lower current than that of 480 ºC cell. $R_s$ is higher for the 460 ºC sample (Table 5.6) and a back barrier is present (which can be seen in dV/dJ plot given in figure A.2 of appendix A). The lower forward current for the 460 ºC sample is due to the back contact. The light J-V (figure 5.9 (bottom)) shows the similar trend. The $V_{oc}$, $FF$, and the $R_{sh}$ are similar in both devices. From the SR in figure 5.10, it can be observed that the 480 ºC sample possibly has a slightly thinner CdS. But this variation is within experimental variations.
5.4 Substrate Temperature

Substrate temperatures are always kept lower than the source temperatures which allows CdCl$_2$ vapor to be available to the substrate before they reach the predetermined temperature. Substrate temperatures were varied from 420°C to 450°C at an increment of 10°C and their effect on average $V_{oc}$ and $FF$ have been investigated.

Samples #2, #3, #11, and #41 have been treated with a source temperature of 460°C while samples #12 and #31 have been treated with 480°C source temperature. The effect of substrate temperature on average $V_{oc}$ and $FF$ has been studied by keeping all the other test conditions such as source temperature, treatment time and CdS thickness constant. Set 1 (sample #2, #3, #11 and #41) and Set 2 (sample #12 and #31) of such similar conditions have been analyzed for varying substrate temperature as shown in Table 5.7 and are plotted in figure 5.11.

It has been observed that at higher source temperature (480°C), the average $V_{oc}$ decreases significantly with increasing substrate temperature while at lower source temperature (460°C), the average $V_{oc}$ decreases gradually with increasing substrate temperature. A similar trend has been found for the $FF$. 
Table 5.7  Samples Annealed at Different Substrate Temperatures

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Set 1</th>
<th>Set 2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>#2</td>
<td>#3</td>
</tr>
<tr>
<td>Treatment time (s)</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>Source temp (°C)</td>
<td>460</td>
<td>460</td>
</tr>
<tr>
<td>Substrate temp (°C)</td>
<td>450</td>
<td>440</td>
</tr>
<tr>
<td>CBD time (min)</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>Max. Avg. $V_{oc}$ (mV)</td>
<td>770</td>
<td>785</td>
</tr>
<tr>
<td>FF (%)</td>
<td>53.1</td>
<td>53.8</td>
</tr>
</tbody>
</table>

It can be seen in the above Table 5.7 that the maximum average $V_{oc}$ of 828 mV and $FF$ of 65% can be obtained at 420° C substrate temperature for sample #12.

Figure 5.11  Average $V_{oc}$ and FF Versus Substrate Temperature
Figure 5.11 shows that the average $V_{oc}$ and $FF$ decrease with 420°C substrate temperature. At 420°C substrate temperature, higher average $V_{oc}$ has been obtained for a source temperature of 480°C, and at 430°C substrate temperature higher average $V_{oc}$ has been obtained at a source temperature of 460°C.

This behavior is believed to be due to the effects of CdCl$_2$ vapor pressure and substrate temperature on the properties of the CdS/CdTe interface.

5.4.1 J-V and SR Analysis

J-V and SR data are shown in figure 5.12 and 5.13 respectively. Table 5.8 shows results of the best devices at different substrate temperatures and table 5.9 shows $R_{sh}$ and $R_s$ for the same devices.
Figure 5.12 Dark J-V (top), Light J-V (bottom) for Sample #2, #3, #41 and #11
Figure 5.13  SR for Different Substrate Temperatures(Sample #2, #3, #11 and #41)

Table 5.8  Cell Results for Samples #2, #3, #41 and #11(T_{SRC}=460°C, t = 90 Seconds)

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>Substrate Temp(°C)</th>
<th>Max. V_{oc} (mV)</th>
<th>FF (%)</th>
<th>J_{sc} (mA/cm²)</th>
<th>Efficiency η(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#2 (4-17-A6-1a)</td>
<td>450</td>
<td>770</td>
<td>57.5</td>
<td>22.64</td>
<td>10.02</td>
</tr>
<tr>
<td>#3 (3-22-A18-2a)</td>
<td>440</td>
<td>790</td>
<td>58.1</td>
<td>22.44</td>
<td>10.30</td>
</tr>
<tr>
<td>#41 (3-23-A2-1a)</td>
<td>430</td>
<td>800</td>
<td>64.1</td>
<td>23.19</td>
<td>11.89</td>
</tr>
<tr>
<td>#11 (4-17-A12-1c)</td>
<td>420</td>
<td>830</td>
<td>67.1</td>
<td>22.81</td>
<td>12.70</td>
</tr>
</tbody>
</table>
Table 5.9  $R_s$ and $R_{sh}$ for Samples Annealed at Different Substrate Temperatures

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Substrate Temp(ºC)</th>
<th>$R_{sh}$ (Ω-cm$^2$)</th>
<th>Dark $R_s$ (Ω-cm$^2$) (upper limit)</th>
<th>Light $R_s$ (Ω-cm$^2$) (upper limit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#2 (4-17-A6-1a)</td>
<td>450</td>
<td>800</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>#3 (3-22-A18-2a)</td>
<td>440</td>
<td>800</td>
<td>10</td>
<td>2</td>
</tr>
<tr>
<td>#41 (3-23-A2-1a)</td>
<td>430</td>
<td>900</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>#11 (4-17-A12-1c)</td>
<td>420</td>
<td>900</td>
<td>7</td>
<td>0.7</td>
</tr>
</tbody>
</table>

The dark ln J-V in figure 5.12 shows a similar $J$ for the #2(450 ºC), #41(430 ºC) and #11(420 ºC) and a higher $J$ for #3(440 ºC). This suggests that the recombination in cell #3 is higher. The reason of this high recombination is not clear since the other high temperature cell (450 ºC sample) shows less recombination. From linear dark J-V it can be observed that there is a curve shift from low to high substrate temperature. This is believed to be due to CdS photoconductivity at the front ($R_s$ is associated with CdS which is difficult to quantify) of the higher substrate temperature samples as shown in figure A.3 of appendix A. The CdCl$_2$ treatment at higher temperatures like 450, 440 ºC may cause an excessive interdiffusion between CdS and CdTe which has a detrimental effect on the cells. This may be the reason for the low $V_{oc}$ (Table 5.8) towards higher substrate temperatures. It can be seen from Table 5.9 that $R_s$ is decreasing with decreasing substrate temperature. The $FF$ depends on $R_s$ and it is increasing with decreasing substrate temperature (Table 5.8). The best $V_{oc}$ and $FF$ are obtained at 420 ºC. However, $J_{sc}$ is higher in 430 ºC due to a thinner CdS as shown in the Q.E. of figure 5.13.
5.5 Treatment Time

The treatment time was varied from 15 seconds to 2 minutes in order to obtain the optimum treatment time of CdCl$_2$ vapor. The treatment time is the time interval from the instant that the cells reached the predetermined annealing temperature until the heaters were turned off. Three different sets of data have been compiled in Table 5.10 to analyze the effect of treatment time on the average $V_{oc}$ and $FF$. From set 1 (#8, #7 and #6) of source/substrate temperature of 480/420°C and of 80 min CBD, it has been found that the average $V_{oc}$ and $FF$ increases with increasing treatment time. From set 2 (#45, #41 and #28), the maximum average $V_{oc}$ has been obtained at 90 sec treatment time. In the case of set 3 (#34 and #31), the average $V_{oc}$ and $FF$ decreases with increasing treatment time (from 30 sec to 90 sec) as shown in figure 5.14. The best overall performance was obtained for 90 sec treatment time and 480/420°C source/substrate temperature. The $FF$’s and average $V_{oc}$’s are plotted in figure 5.14.
Table 5.10  Samples Annealed at Different Treatment Times

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Set 1</th>
<th>Set 2</th>
<th>Set 3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>#6</td>
<td>#7</td>
<td>#8</td>
</tr>
<tr>
<td>#45</td>
<td>#41</td>
<td>#28</td>
<td></td>
</tr>
<tr>
<td>#31</td>
<td>#34</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Treatment time (s)</th>
<th>90</th>
<th>60</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>30</td>
<td>90</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>90</td>
<td>30</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Source temp (°C)</th>
<th>480</th>
<th>480</th>
<th>480</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>460</td>
<td>460</td>
<td>460</td>
</tr>
<tr>
<td></td>
<td>480</td>
<td>480</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Substrate temp (°C)</th>
<th>420</th>
<th>420</th>
<th>420</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>430</td>
<td>430</td>
<td>430</td>
</tr>
<tr>
<td></td>
<td>430</td>
<td>430</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CBD time (min)</th>
<th>80</th>
<th>80</th>
<th>80</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>90</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td></td>
<td>90</td>
<td>90</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Max. Avg. $V_{oc}$ (mV)</th>
<th>800</th>
<th>790</th>
<th>780</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>775</td>
<td>787.5</td>
<td>780</td>
</tr>
<tr>
<td></td>
<td>770</td>
<td>782.5</td>
<td></td>
</tr>
</tbody>
</table>

| FF (%) | 62.2 | 60.6 | 55.3 | 65.3 | 60 | 55.5 | 59.6 | 61.4 |

Voc - 480/420°C, 80 min CBD (#8, #7, #6)
Voc - 460/430°C, 90 min CBD (#45, #41, #28)
Voc - 480/430°C, 90 min CBD (#34, #31)
FF - 480/420°C, 80 min CBD (#8, #7, #6)
FF - 460/430°C, 90 min CBD (#45, #41, #28)
FF - 480/430°C, 90 min CBD (#31, #34)

Figure 5.14  Average $V_{oc}$ and FF Versus Treatment Time
5.5.1 J-V and SR Analysis

The J-V and SR data for the samples of Table 5.11 are shown in figures 5.15 and 5.16 respectively. Table 5.11 shows the results of the best devices and Table 5.12 shows $R_s$ and $R_{sh}$ for the same samples.

Table 5.11 Cell Results for Samples #6, #7, and #8 ($T_{SRC}$=480°C, $T_{SUB}$=420°C)

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>Treatment Time (sec)</th>
<th>$V_{oc}$ (mV)</th>
<th>FF (%)</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>Efficiency η(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#6 (4-17-A20-1d)</td>
<td>90</td>
<td>800</td>
<td>62.6</td>
<td>23.50</td>
<td>11.76</td>
</tr>
<tr>
<td>#7 (4-17-B20-1a)</td>
<td>60</td>
<td>790</td>
<td>62.3</td>
<td>23.12</td>
<td>11.38</td>
</tr>
<tr>
<td>#8 (4-17-A21-2d)</td>
<td>15</td>
<td>780</td>
<td>58.4</td>
<td>22.94</td>
<td>10.45</td>
</tr>
</tbody>
</table>

Table 5.12 $R_s$ and $R_{sh}$ for Samples Heat Treated at Different Treatment Times

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Treatment Time(sec)</th>
<th>$R_{sh}$ (Ω-cm$^2$)</th>
<th>Dark $R_s$ (Ω-cm$^2$) (upper limit)</th>
<th>Light $R_s$ (Ω-cm$^2$) (upper limit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#6 (4-17-A20-1d)</td>
<td>90</td>
<td>800</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>#7 (4-17-B20-1a)</td>
<td>60</td>
<td>900</td>
<td>2</td>
<td>1.5</td>
</tr>
<tr>
<td>#8 (4-17-A21-2d)</td>
<td>15</td>
<td>900</td>
<td>11</td>
<td>4</td>
</tr>
</tbody>
</table>
Figure 5.15  Dark J-V (top), Light J-V (bottom) for Sample #6, #7, and #8
Figure 5.16  SR Curves for Different Treatment Times (Samples #6, #7, and #8)

The dark ln J-V in figure 5.15 shows small variations in the dark current below 0.8 volt for all three treatment times. From the linear J-V it can be seen that 15 sec sample (#8) exhibits a higher $R_s$, and there is a back contact barrier which can be seen in the $dV/dJ$ plot given in figure A.4 of appendix A. Therefore the low $FF$ of this sample is due to the back contact. The low $V_{oc}$ of #8 may also be due to the back contact barrier. 90 sec treatment time exhibits the best performance for all the samples.
CHAPTER SIX

CONCLUSION

The average performance of the solar cells (in terms of $V_{oc}$ and $FF$) decreases towards the rear end of the substrate holder, more prominently at lower source temperatures of 460°C. Better uniformity in devices from front to rear of the substrate holder can be achieved by increasing the source temperature up to 480°C.

A relationship can be observed between the source and the substrate temperature while obtaining higher $V_{oc}$ and $FF$. If the source temperature of CdCl$_2$ vapor chamber is higher (i.e. 480°C in this study), the substrate temperature should be lower (i.e. 420°C) and vice versa. Based on the results obtained in this thesis it is apparent that both the substrate annealing temperature and the amount of CdCl$_2$ are affecting device performance and must be optimized together. To better understand this process, detailed analysis of the interface is necessary.

With regard to the treatment time, it can be concluded that the optimum time to obtain maximum average $V_{oc}$ and $FF$ varies with source/substrate temperatures. Shorter treatment time is desirable for a higher source/substrate (480/430°C) temperature combination, while longer time is required for high/low (480/420°C) and low/high (460/430°C) source/substrate combinations.
The conditions for the best device in this research are source temperature = 480°C, substrate temperature = 420°C, treatment time = 90 sec, He/O₂ = 160/40 cc, and CBD time for CdS = 90 min.

The cell parameters obtained for the best device are V_{oc} = 830 mV, FF = 65%, J_{sc} = 23.53 mA/cm², and η = 12.69%.
REFERENCES


Appendix A: Test Results of Series and Shunt Resistance

Figure A.1 Series and Shunt Resistance for Position # 2

Figure A.2 Series and Shunt Resistance for Source Temperature 460°C
Appendix A (Continued)

Figure A.3  Series and Shunt Resistance for Substrate Temperature 440 °C

Figure A.4  Series and Shunt Resistance for Treatment Time 15-sec