Growth of 3C-SiC via a Hot-Wall CVD Reactor

by

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GROWTH OF 3C-SiC VIA A HOT-WALL CVD REACTOR

Suzie Harvey

ABSTRACT

The heteroepitaxial growth of cubic silicon carbide (3C-SiC) on silicon (Si) substrates at high growth rates, via a horizontal hot-wall chemical vapor deposition (CVD) reactor, has been achieved. The final growth process was developed in three stages; an initial “baseline” development stage, an optimization stage, and a large area growth stage. In all cases the growth was conducted using a two step, carbonization plus growth, process. During carbonization, the surface of the Si is converted to 3C-SiC, which helps to minimize the stress in the growing crystal. Propane (C$_3$H$_8$) and silane (SiH$_4$), diluted in hydrogen (H$_2$), were used as the carbon and silicon source, respectively. A deposition rate of approximately 10 μm/h was established during the baseline process. Once the baseline process proved to be repeatable, optimization of the process began. Through variations in temperature, pressure, and the Si/C ratio, thick 3C-SiC films (up to 22 μm thick) and high deposition rates (up to 30 μm/h) were obtained. The optimized process was then applied to growth on 50 mm diameter Si(100) wafers. The grown 3C-SiC films were analyzed using a variety of characterization techniques. The thickness of the films was assessed through Fourier Transform infrared (FTIR) spectroscopy, and confirmed by cross-section scanning electron microscopy (SEM). The SEM cross-sections were also used to investigate the 3C-SiC/Si interface. The surface morphology of the films was inspected via Nomarsky interference optical microscopy, atomic force
microscopy (AFM), and SEM. The crystalline quality of the films was determined through X-ray diffraction (XRD) and low-temperature photoluminescence (LTPL) analysis. A mercury probe was used to make non-contact CV/IV measurements and determine the film doping.
CHAPTER 1 INTRODUCTION

1.1 3C-SiC Overview

Silicon carbide has been heralded as a promising candidate to replace silicon for power device applications due to its large band gap and high electron mobility. Its mechanical strength and robust nature make it an ideal material for military applications in harsh environments. Unlike Si based devices, which can only operate up to 200 °C, SiC devices have been shown to operate effectively at temperatures up to 600 °C [1]. SiC forms in more than 170 known polytypes, or crystal structures. However, 95% of all publications concerning SiC deal primarily with the polytypes 4H-, 6H-, and 3C-SiC [2]. The designations denote the structure of the crystal as being either cubic or hexagonal (Figure 1.1). In the case of 3C-SiC, the cubic crystal repeats three times to comprise the unit cell.

![Stacking order of a few commonly studied SiC polytypes](image)

Figure 1.1: Stacking order of a few commonly studied SiC polytypes [3].
This thesis focuses on the growth of the only purely cubic polytype, 3C-SiC. The advantage of 3C-SiC over the more commonly studied hexagonal polytypes (6H- and 4H-SiC), is its ability to be hetero-epitaxially grown on Si, providing a cost effective alternative to homo-epitaxy on bulk SiC. Bulk SiC is expensive, approximately $1500-$2000 per wafer, and is currently only available commercially in a maximum diameter of 4 inches [4]. At this time, 3C-SiC bulk crystals are not commercially available. However, Si wafers are inexpensive and are manufactured as large as 12 inches. In theory, 3C-SiC could be epitaxially grown on large-area Si wafers to produce seeds for bulk growth. Additionally, bulk SiC contains screw dislocations that can penetrate into the epitaxial layer during growth. Because Si can be manufactured as nearly defect free, these dislocations can be eliminated in 3C heteroepitaxy.

However, despite the advantages there exist many challenges to the successful heteroepitaxy of 3C-SiC on Si. One is the difference in lattice constants between 3C-SiC and Si, which is approximately 20%. The lattice constant or space between atoms for Si is approximately 5.43 Å [5], whereas for 3C-SiC it is 4.36 Å [2]. Because the substrate is thicker than the epitaxial layer, the lattice misfit causes all of the strain to be accommodated in the epilayer, which leads to shear stresses in the crystal planes. Often the bonds along these planes will break and reform to relieve stress, leaving behind dangling bonds which are referred to as misfit dislocations [6]. Further information on crystallographic defects and the methods of reducing and eliminating them can be found in section 2.2. Another disadvantage of heteroepitaxy is the difference in thermal expansion coefficients between 3C-SiC and Si (see Table 1.1). At the higher temperatures typically used for growth (1350 °C-1400 °C), this difference becomes
smaller [2,5]. These are a few of the issues that must be addressed before 3C-SiC can be realistically considered as a replacement for Si based electronic devices.

1.2 3C-SiC Applications

The thermal, electrical, and mechanical properties of 3C-SiC make it a promising candidate in device fabrication. Table 1.1 compares some of the basic electrical and thermal properties of 3C-, 4H-, 6H-SiC, and Si. What makes 3C-SiC based devices more appealing than Si is its ability to function at higher voltages, higher frequencies, and higher temperatures.

Table 1.1: Basic electrical and thermal properties of 3C, 4H, 6H SiC and Si [2,5,7].

<table>
<thead>
<tr>
<th></th>
<th>3C-SiC</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap Eg (eV)</td>
<td>2.4</td>
<td>3.2</td>
<td>3.0</td>
<td>1.12</td>
</tr>
<tr>
<td>Mobility (\mu_n) (cm(^2)/v*s)</td>
<td>1000</td>
<td>950</td>
<td>500</td>
<td>1350</td>
</tr>
<tr>
<td>Sat. drift V (x10(^7) cm/s)</td>
<td>2.5</td>
<td>2.0</td>
<td>2.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Thermal cond. (W/cm K)</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
<td>1.5</td>
</tr>
<tr>
<td>Thermal expansion @300 K</td>
<td>3.8</td>
<td>NA</td>
<td>4.3 (\perp c) axis</td>
<td>2.6</td>
</tr>
<tr>
<td>@1500-1600 K (10(^6) K(^{-1}))</td>
<td>5.5</td>
<td>NA</td>
<td>4.7 (\parallel c) axis</td>
<td>4.56-4.6</td>
</tr>
</tbody>
</table>

For high voltage devices, SiC can handle about ten-times the critical electric field for Si, which means a lower on-resistance for the same blocking voltage [7]. For example, power MOSFETs have better output characteristics for paralleling devices than BJTs, and the high input impedance allows for simpler gate drive circuitry. Unfortunately, the advantage is lost with a Si power MOSFET, due to the high on-resistance for high breakdown voltages. An ideal 3C-SiC power MOSFET operating at
room temperature, for a breakdown voltage of 5 kV, has a specific on-resistance which is three orders of magnitude smaller than for a similar Si device [8]. High frequency devices also benefit from the high critical field of SiC, because it allows for smaller and therefore faster devices [7]. From Table 1.1, we can see that 3C-SiC has a larger saturated drift velocity than both 4H- and 6H-SiC polytypes, and is more than twice that of Si, which is advantageous for obtaining higher channel currents in microwave devices [9]. Additionally, of the three SiC polytypes shown in Table 1.1, 3C-SiC has the highest electron mobility. The carrier mobility influences the frequency response or time response behavior of a device in two ways. First, the mobility is proportional to the carrier velocity for low electric field. Therefore a higher mobility material is likely to have a higher frequency response, because carriers can move more readily through the device. Second, the device current is dependant on the mobility; i.e. higher motilities result in larger currents. At larger currents, the capacitance will charge more rapidly, which will result in a higher frequency response [10].

At high temperatures, SiC also holds the advantage over Si. The failure of Si devices at high temperatures is mostly attributed to the thermal ionization of electrons from the valence band to the conduction band [9]. The ionization of a large number of electrons into the conduction band causes the material to become intrinsic; meaning there is no longer a p-n junction to block the voltage in, say, a bipolar device [7]. Because of the large bandgap, SiC has a much higher intrinsic temperature and does not suffer the same fate; SiC devices have been shown to operate effectively up to 600 °C, while most Si based devices fail at around 200 °C [1]. The ability to operate at high temperatures is a major advantage for military and space applications. Researchers at NASA’s Glenn
Research Center believe SiC technology will reduce satellite launch costs by eliminating the need for bulky cooling radiators, allow future missions into harsh environments (e.g. Venus’ 450 °C atmosphere), and provide high temperature sensors and control electronics in aircraft and automobiles [11]. Closer to home, hydrogen fuel cell research at the University of South Florida has led to the successful fabrication of 3C-SiC based H$_2$ gas sensors [12], further motivating the research performed during this thesis.

The benefits of 3C-SiC and SiC research span across a vast number of disciplines; from power electronics to chemical sensors to medical applications and biotechnology. As bulk and epitaxial SiC growth processes continue to improve, so too will the many applications for which they are used since this is the key limiting factor for SiC technology insertions.

1.3 Summary

SiC is a robust material with electrical, mechanical, and thermal advantages over Si. The quality of 6H- and 4H-SiC bulk crystals and epitaxy continues to improve towards device grade material, and Intrinsic Semiconductor, now part of Cree Inc [4], has reported the development of micropipe-free and low density (1 cm$^{-2}$) 100 mm 4H- and 6H-SiC wafers[4]. However, problems continue to plague this technology, with no serious reductions in screw dislocations in 4H- and 6H-SiC. 3C-SiC heteroepitaxy on Si does not suffer from these inherent problems, which is the main motivation besides cost reduction, for using this material. Nonetheless, 3C-SiC technology must overcome its own limitations arising from process instability, defects, and a lack of interest/research. Therefore, it is the goal of this thesis to investigate the growth of 3C-SiC on Si via Hot-wall CVD epitaxy, improve upon the current crystal quality, and apply these advances for
useful applications. In Chapter 2, the basic theory of CVD will be discussed since this is the primary method used to grow 3C-SiC. In addition, common defects found in the heteroepitaxy of 3C-SiC on Si will be presented along with a review of the literature concerning recent developments and methods of 3C-SiC heteroepitaxy. In Chapter 3, the development of a 3C-SiC on Si growth process in a hot wall CVD reactor will be presented, where growth rates up to 30 μm/h and whole wafer films up to 22 μm thick were achieved. Also, the results of several characterization methods used to analyze the grown films will be discussed. In Chapter 4, several applications for which we are using the grown 3C-SiC epitaxial layers will be discussed, namely, growth on wafer bonded films (SOI), MOSFETs, and MEMS. Finally, the thesis will conclude with a discussion of the work performed during this research, and future projects which are the logical extension of this work.
CHAPTER 2  3C-SiC HETEROEPITAXY

2.1 Epitaxy

Epitaxy is the layered growth of a crystalline film on a crystalline substrate [13]. The substrate acts as the seed crystal, and therefore its structure influences the growing crystal due to a degree of matching at the interface between the two [6]. In homoepitaxy, the lattice parameter of the deposited material matches that of the substrate, and the film/substrate interface should vanish into the bulk material so that the interface energy, $\gamma_i$, is approximately zero [6,13]. In heteroepitaxy, the deposited material has a different lattice parameter than the substrate. The epitaxial film orients itself to minimize $\gamma_i$ and maximize bonding at the interface [6]. If the difference in lattice parameters is too great, epitaxy is not possible [13]. The fractional mismatch, $f$, at the interface should be relatively small ($f < 0.1$), and is defined as:

$$f = \frac{(a_e - a_s)}{(a_e + a_s)/2} \approx \frac{(a_e - a_s)}{a_s}$$  \hspace{1cm} (2.1)

where $a_e$ and $a_s$ are the atomic spacing’s of the epitaxial film and substrate, respectively [6]. If there is a difference in thermal expansion coefficients between the two materials, then $f$ becomes a function of temperature, as in the case of 3C-SiC on Si [6]. Because the substrate acts as a seed for the epitaxy, the structure of its surface is important in determining the growth mechanism. If the surface is atomically smooth, the rate of growth is determined by two independent processes: (i) the formation of steps, and (ii) the lateral movement of these steps [14]. In vapor phase epitaxy (VPE), the following
mechanisms contribute to the overall growth process: (1) the atoms from the vapor adsorb onto the step terraces, which creates a population of adatoms, (2) the surface diffusion of the adatoms towards the step edges, (3) the adatoms incorporate along the kinks in the steps, which leads to the lateral movements of the steps, and contributes to the growth of the crystal. If dislocations are present in the crystal, growth is no longer determined by step formation but instead it is influenced by other factors, such as the rate of surface diffusion, interaction between steps, encounters with surface defects and impurities, etc. [14].

2.1.1 CVD epitaxy

A common technique used to grow crystalline films epitaxially is chemical vapor deposition (CVD), which is a type of VPE. The types of CVD include: thermal CVD, such as low pressure (LPCVD) and atmospheric pressure (APCVD), and plasma enhanced (PECVD). CVD is controlled by two basic process; mass transfer, and surface reaction [15]. These two processes can be broken down into a sequence of five steps. The reactant gas molecules or precursors, diluted in a carrier gas, are introduced into the reaction chamber, where: (1) The gases diffuse through a boundary layer to the surface, (2) the reactants adsorb to the surface, (3) a chemical reaction takes place, resulting in deposition, (4) the adsorbed species are desorbed, and (5) the by-products of the reaction are diffused out [13]. For example, during 3C-SiC CVD, propane and silane thermally decompose and form C and Si subspecies, which then adsorb to the heated Si surface, resulting in a 3C-SiC epitaxial layer. Many variables must be taken into consideration in order for CVD epitaxy to be successful, such as, reactor design, gas chemistry, and process parameters. For instance, the temperature and pressure inside the reactor greatly
affect the deposition process. The pressure controls the thickness of the boundary layer and therefore determines the amount of diffusion that can occur [13]. At low pressures, the boundary layer is thinner, which minimizes the diffusion process. This is known as a surface controlled regime; where the rate of deposition is limited by the reaction at the surface [13,16,17]. If temperature is low, the molecules react slowly and create an oversupply [18]. If temperature is high, the molecules react quickly on the surface and the deposition is then limited by the diffusion (transport) of the molecules through the boundary layer [17]. The growth regime (transport-limited or surface reaction-limited) is determined by the slowest process (diffusion or reaction) [13]. Figure 2.1 illustrates how both the temperature and pressure during CVD affects the growth rate.

![Figure 2.1: Overall reaction rate vs. reciprocal temperature for CVD [6,16].](image)

In a horizontal CVD reactor, the boundary layer increases along the x direction, which leads to an exponential decrease in the deposition. A tilted susceptor design is often employed to increase the gas velocity, and thus reduce the boundary layer [17].
Figure 2.2 (a) and (b) illustrate how the tilted susceptor design not only helps to reduce the boundary layer, but also improves deposition uniformity.

Figure 2.2: Illustration of boundary layer $\delta$ in horizontal reactor with: (a) flat susceptor design, and (b) tilted susceptor design [13,17].

In PECVD, the growth mechanisms are similar to that of thermal CVD, with the addition of a plasma to assist in the deposition process. A plasma is a partially ionized gas that when subjected to an applied electric field the electrons can achieve higher energies than atoms and molecules. This results in more free radicals by electron bombardment than would be possible thermally [17]. The free radicals have a high chemical reactivity which allows for nucleation at a much lower temperature than what is required for thermal reaction [6]. There are two main reasons plasma CVD is used rather than thermal CVD. The first is the ability to crack the same molecules at lower temperatures, which is a necessity for many integrated circuit (IC) technologies. In fabricating ICs, silicon nitride (SiN) is often deposited as a final passivation layer, which if deposited thermally, would require a temperature of 750 °C. However, most metal contacts are aluminum (Al), which melts at approximately 600 °C. If a plasma is used, SiN can be deposited below 500 °C and damage to the contacts can be avoided [6,17,18]. The second reason for using plasmas is that the film surface becomes denser due to the increase in ion bombardment. This gives one the ability to adjust the density, and therefore stress, in a film through the manipulation of process conditions [18].
2.1.2 3C-SiC epitaxy

The most common technique used to grow 3C-SiC epitaxially is CVD [7,9]. The epitaxial growth of 3C-SiC on Si has been achieved using atmospheric pressure, low pressures, and even a combination of both. Refer to section 2.3 for more details on the variety of growth processes in use. Typically a two stage growth process, first developed by Nishino et. al [19], is used for 3C-SiC heteroepitaxy. Growth has been achieved with some success when the carbonization step was omitted [20], but this usually resulted in lower quality films [21-23]. In the first stage, a carbonization of the surface is performed using a hydrogen-hydrocarbon gas mixture. The carbonization step converts the surface of the Si substrate to SiC, which serves as a quasi buffer layer for the epitaxial growth [19]. In the second stage, a silicon source precursor is added to the gas mixture and the primary growth takes place. The more commonly used carbon and silicon sources are propane (C$_3$H$_8$) and silane (SiH$_4$), respectively. Simulations of 4H-SiC growth in a horizontal hot-wall CVD reactor (same reactor used for the 3C-SiC growth presented in this thesis) performed by Shishkin et. al [24], found that the primary C and Si species contributing to growth were CH$_4$, SiH$_2$ and Si. Other species, such as C$_3$H$_8$ and SiH$_4$ as well as C$_2$H$_5$, C$_2$H$_2$, and CH$_3$ likely give negligible contributions to the growth due to their small presence in the growth zone. Although the simulation parameters were established for 4H-SiC homoepitaxy, the propane/silane precursor chemistry is similar to that used for 3C-SiC hereroepitaxy.

2.2 Defects in 3C-SiC Epitaxy

Impurities and defects can cause disruptions in the deposition of films because the arriving atoms need to sense the crystallographic order of the underlying substrate.
Therefore, surface structure is important for controlling defects and obtaining charge neutrality at the interface during heteroepitaxy. A significant difference in charge can produce large electrostatic fields which disrupt smooth growth [6]. There are several defects typically associated with 3C-SiC heteroepitaxy; planar defects, such as stacking faults (SFs) and anti-phase boundaries (APBs), and other defects, such as interface voids and hillocks [20,25,26].

2.2.1 Planar defects

A major contributor to the defects in heteroepitaxy is the lattice mismatch and difference in thermal expansion coefficients between 3C-SiC and Si, which is approximately 20% and 8%, respectively [25,27,28]. The misfit causes stress in the epilayer which can lead to dislocations in the crystal structure [6]. Misfit dislocations occur when the crystal plane breaks to relieve stress, leaving behind dangling bonds. The lattice mismatch also forces the crystal to grow as three-dimensional islands, known as island growth mode [25]. Each island has a slightly different orientation and as neighboring islands coalesce, the periodicity of the lattice is broken, creating an APB or grain boundary [29]. At the interface between two APBs, there is an exchange of Si and C atoms in an effort to minimize the number of dangling bonds, resulting in Si-Si or C-C bonds (twins) along the planes [26]. The inversional stacking of the Si and C bilayers introduces parasitic hexagonal phases within the 3C-SiC films. These errors in stacking sequences are known as stacking faults (see Figure 2.3). In 3C-SiC heteroepitaxy, it is energetically favorable for small misfits in the crystal lattice to be accompanied by SFs, because the lattice spacing of the parasitic hexagonal (0006) plane and the cubic (111) plane are similar [29]. SFs and APBs are two of the primary defects influencing the
electrical properties and therefore performance of devices [20,29]. They are thought to be the origin of current leakage when they penetrate the p-n junction [26], and SF’s also act as recombination centers for carriers in bipolar devices [9]. Yun et. al [25] and Zheng et. al [29] both found a direct correlation between the size of the crystallites and the number of SFs; thicker epi films lead to larger crystallites and fewer planar defects.

Many different techniques have been employed to try and reduce the strain in the 3C-SiC epilayer caused by the lattice mismatch, such as, growth on undulant-Si [26] or on porous substrates [31,32]. The carbonization step performed prior to growth also helps to reduce the strain at the 3C-SiC/Si interface. The carbonization converts the surface layer of Si to 3C-SiC, and acts as a quasi buffer layer for the subsequent growth [19]. Unfortunately, carbonizing the Si surface has been found to contribute to the formation of voids at the film/substrate interface [27].

2.2.2 Voids

It is generally believed that voids are caused by the out-diffusion of Si atoms from the substrate, which reacts with carbon in the vapor phase to form SiC during the carbonization [27,33,34]. However, Leycuras proposed voids could be caused by the
formation of carbon monoxide from the carbon reacting with oxygen impurities in the Si substrate [35]. Voids form as inverted pyramids at the 3C-SiC/Si interface and are bridged by the growing SiC layer [28]. There are many techniques used to reduce or eliminate voids at the interface. Nagasawa et. al [36] and Chiu et. al [37] used only hydrocarbon sources during carbonization, such as C$_2$H$_4$ and C$_2$H$_2$, to suppress void formation. Burkland et. al [27] used the addition of SiH$_4$ during carbonization to suppress the out-diffusion of Si by providing an alternative Si source for the C to react with. Seo et. al [34] were able to achieve void-free interfaces by employing low temperature nucleation with tetramethylsilane (TMS) prior to high temperature growth. Other researchers have varied process conditions such as ramp times, temperature, and pressure to obtain void-free interfaces [38-40].

2.2.3 Hillocks

Another defect in 3C-SiC heteroepitaxy which becomes more prominent at higher growth rates, is hillocks [20]. Hillocks are surface protrusions that have a negative impact on the surface morphology of a 3C-SiC film. Not much information can be found in the 3C-SiC growth literature on the cause of hillock formation, nor on their point of origination. However, in section 3.3.3, this thesis will present results of an investigation into the nature of these defects, from which the following conclusions can be drawn: (1) as the thickness of the film increases, the defects appear to increase in size and density, and (2) hillocks are more pronounced along the edges of the samples, where defects are more abundant in the underlying substrate due to dicing. This is one reason why growth on larger areas is necessary to increase the amount of usable surface area.
2.3 Review of 3C-SiC Growth Literature

Although SiH$_4$ and C$_3$H$_8$ are most often used as the Si and C sources for 3C-SiC heteroepitaxy [7], there are many different types of precursor chemistries that have been successfully used, such as single source metal organics and chlorine additives.

2.3.1 Single source precursors

Hexamethyldisilane [(CH$_3$)$_6$Si$_2$], or HMDS, is an organometallic precursor that can be used as the sole source for both Si and C. Because HMDS has a pre-existing Si-C bond, growth can be achieved at lower temperatures [33]. HMDS is incorporated into the deposition process by using the metal organic (MO) CVD technique. In MOCVD, the source material is in liquid form and is held in a separate container usually maintained at room temperature. The vapor phase species are transported into the reaction chamber by bubbling a carrier gas, such as H$_2$, through the liquid. The reactants then thermally decompose when coming into contact with the hot susceptor. The advantage of using MOCVD is that deposition is not diffusion limited, as is the case with other CVD processes [41]. Gupta et al [33] was able to achieve single crystal 3C-SiC films on Si(100) and (111) substrates using H$_2$ bubbled through HMDS as a sole source. The carbonization step was performed prior to growth using C$_3$H$_8$. Growth was conducted for 1-2 hours at temperature between 1150 °C and 1250 °C. Teker et al [21] also conducted growth experiments on Si(100) and (111) using HMDS. However, they used an Ar/H$_2$ carrier mix and omitted the carbonization step in favor for a nucleation stage. The nucleation stage took place at 1250 °C for 2 minutes with an HMDS flow of 1.25 sccm. Growth took place at 1380 °C with HMDS flow rates between 0.625 and 5 sccm. They reported the films to have a high density of planar defects and voids at the substrate/epi...
Trimethylsilane [(CH$_3$)$_3$SiH], or 3MS, has also been used as a single source in 3C-SiC heteroepitaxy. Madapura et. al [22] was able to achieve high growth rates (up to 35 $\mu$m/h), with and without the carbonization step, using 3MS. They found the growth rate to be highly dependant on temperature and the non-carbonized samples had higher growth rates, but lower quality films. The advantage of 3MS over the traditional silane/propane precursor chemistry is its non-corrosive, non-pyrophoric properties.

2.3.2 Chlorine additives

The addition of chlorines in 3C-SiC CVD epitaxy has gained recent interest, due to its apparent ability to help suppress the homogeneous nucleation of Si in the gas phase [42,43]. Wang et. al [44] was able to deposit 3C-SiC epitaxially at low temperatures (750 °C-900 °C), using dichlorosilane (SiH$_2$Cl$_2$) and acetylene (C$_2$H$_2$). However, the deposited films were amorphous at 750 °C and highly grainy at 900 °C. Here at the University of South Florida, M. Reyes et. al [42] has achieved growth rates up to 38 $\mu$m/h with the addition of HCl to the C$_3$H$_8$/SiH$_4$ precursor chemistry. The 3C-SiC layers were deposited on Si(100) substrates at temperatures between 1370 °C-1380 °C. The resulting films were single-crystalline and specular. The addition of HCl has also helped to achieve growth of 3C-SiC on Si at lower temperatures. However, the growth rates are much lower and the quality not yet comparable to the films grown at higher temperatures [45].

2.4 Summary

Chemical vapor deposition is a common technique used to grow crystal films epitaxially. CVD is governed by two basic mechanisms; mass transfer and surface
reaction [15]. Reactant gas molecules, or precursors, diluted in an inert carrier gas such as H\textsubscript{2} or Ar, are injected into the CVD reaction chamber, where they diffuse through a boundary layer and chemically react with the surface to create an epitaxial layer. Many variables must be taken into consideration in order for CVD epitaxy to be successful, such as the temperature and pressure inside the reactor. At lower chamber pressures, the boundary layer thickness is reduced and deposition is more uniform [13]. At higher temperatures, surface reaction is quicker and deposition rates are higher [17]. If the depositing film and substrate have matching lattice parameters, then the growth is said to be homoepitaxial. If the lattice parameters are different, then the growth is said to be heteroepitaxial, as in 3C-SiC growth on Si.

In 3C-SiC CVD, precursor molecules containing Si and C elements, thermally decompose and adsorb to the heated Si surface to form a heteroepitaxial layer of 3C-SiC. There are many different precursor chemistries used in 3C-SiC epitaxy, such as propane and silane (the most common), hexamethyldisilane (used as single source for both C and Si) and hydrochloride (used as chlorine additive), each with their own advantages and disadvantages. Yet despite the variety of processes available, there are still many defects associated with 3C-SiC heteroepitaxy. Some defects, such as APBs, SFs, and twins, are caused by strain in the crystal planes due to the lattice mismatch between 3C-SiC and Si [25,26,29]. Other defects, such as interface voids, are caused by the outdiffusion of Si from the substrate, which reacts with the gas phase carbon source [27,33,34]. The researcher must minimize these defects, through CVD reactor design, gas chemistry and process parameter modification, before epitaxially grown 3C-SiC can be considered as a viable alternative to Si based devices.
CHAPTER 3  3C-SiC CVD PROCESS DEVELOPMENT

3.1 CVD Reactor System Review

The reactor used in this work was a horizontal hot-wall CVD reactor. Figure 3.1 is a photograph of the CVD reactor used, which was built by the SiC group at the University of South Florida [46]. The chamber consists of a quartz tube supported by stainless steel endplates which are water cooled. The gas lines connect to the head of the tube and pass though a gas diffuser cap, similar to a shower head, which helps to disperse the gases and establish laminar flow. An inner quartz liner funnels the gases into the hot zone. The copper coils, shown in Figure 3.1, provide radial heating of the hot zone through radio frequency (RF) induction. A 50 kw/10 kHz Mesta Electronics Inc. [47] solid state RF generator provides the source for the RF induction and is capable of producing temperatures inside the hot zone in excess of 1800 °C. A pyrometer is mounted on the outside of the chamber housing and is aimed at a machined recess in the top portion of the hot zone. Infrared imaging allows the user to determine the temperature inside the hot zone and regulate it through a feedback control loop via a computer interface. The hot zone consists of either silicon carbide or tantalum carbide coated graphite parts, which are called susceptors, and an insulating graphite foam support. The top susceptor was designed with a downward tilt toward the outlet of the gas stream (see Appendix A); this was done to increases the gas velocity, which reduces the boundary layer and leads to more uniform deposition [17].

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The graphite foam helps prevent radiation losses to maintain temperature uniformity, which in turn improves the uniformity of the epitaxial growth. The gas flow is controlled through mass flow controllers (MFCs). A computer program written in Labview™ [48] allows the user to specify gasses and flow rates.

The current reactor configuration is capable of running propane (C₃H₈), silane (SiH₄), hydrochloride (HCl) and methylchloride (CH₃Cl) precursors, nitrogen (N₂) as a doping gas, and argon (Ar) or hydrogen (H₂) as carriers. H₂ is primarily used as the carrier gas and is delivered through a palladium purifier to remove all gas contaminants. The pressure in the chamber is regulated through a control valve and dry vacuum pump, and is capable of maintaining pressures from 70 Torr to 760 Torr, depending on the gas load.

3.2 Process Development

The 3C-SiC heteroepitaxial process described in this chapter was developed in several stages. The initial process began from the research started by R.L. Meyers in her
thesis work [31]. Once a stable growth process that yielded specular films was achieved, optimization of that process began. The goal was to improve the growth rate and crystalline quality in order to produce thick films for power device applications. In the final stage, modifications were made to the CVD reactor and the optimized process applied to growth on 50 mm diameter Si wafers.

3.2.1 Initial “baseline” process

The 3C-SiC on Si growth process was developed using the two step carbonization and growth method described in Chapter 2. C$_3$H$_8$ and SiH$_4$ were used as the precursor gases to provide the carbon and silicon sources, respectively. Ultra high purity (UHP) hydrogen, purified in a palladium diffusion cell, was employed as the carrier gas. The substrates used in the experiments were 8 mm x 10 mm die of n-type Si(100). Prior to growth, the samples were prepared using the standard RCA cleaning method [49], followed by a 30 second immersion in diluted hydrofluoric acid (HF), to remove surface contaminants and the native oxide. The first stage of the process, known as the carbonization step, involved heating the reactor from room temperature to 1140 °C in a C$_3$H$_8$ and H$_2$ only environment at atmospheric pressure. The temperature was then maintained for two minutes to carbonize the surface of the substrate. Experiments performed by R.L. Myers-Ward and M. Reyes on the same CVD reactor, determined the ideal carbonization conditions were at atmospheric pressure with a gas flow of 6 standard cubic centimeters per minute (sccm) of C$_3$H$_8$ and 10 standard liters per minute (slm) of H$_2$ [50]. After carbonization, SiH$_4$ was introduced into the system at 4 sccm and the temperature increased to growth temperatures. A series of experiments were then
conducted to determine the ideal conditions for growth, which included variations in temperature, silicon to carbon (Si/C) ratio, and pressure.

The initial growth conditions previously developed by R.L. Myers-Ward and M. Reyes were as follows: The precursor flows were set to 6 sccm for C$_3$H$_8$, 8 sccm for SiH$_4$, and 30 slm for H$_2$; the temperature set to 1375 °C; the pressure set to 200 Torr. For each set of experiments only one variable was changed at a time. First, the temperature experiments were conducted in the range from 1355 °C to 1385 °C with the best morphology occurring in the range from 1375 °C to 1385 °C. Next, the chamber pressure was varied from 100 Torr to 400 Torr with the best film occurring at 100 Torr. Once the ideal temperature and pressure were established, the flow of C$_3$H$_8$ was fixed and the amount of SiH$_4$ systematically increased. The maximum SiH$_4$ flow achieved, that still resulted in a specular film, was 13 sccm. The resulting Si/C ratio was calculated to be 0.72 and the growth rate measured to be approximately 10 μm/h. Details of the process schedule can be found in Figure 3.2 below.

Figure 3.2: 3C-SiC initial process schedule.
3.2.2 Optimized process

Once the baseline 3C-SiC process had been developed, efforts continued to improve the growth rate and morphology of the epitaxial films. The sample preparation was performed in the manner described in the previous section. The carbon source was the 100% C\textsubscript{3}H\textsubscript{8} used in the initial process, however, the silicon source was replaced with a 10% SiH\textsubscript{4} in H\textsubscript{2} mixture. For all the subsequent experiments, the flow rates were fixed at 10 slm of H\textsubscript{2} and 6 sccm of C\textsubscript{3}H\textsubscript{8} during the initial temperature ramp, two minute carbonization step, and the second temperature ramp to the growth step. Because SiH\textsubscript{4} is introduced into the reaction chamber immediately after carbonization, deposition starts to occur during the second ramp, albeit at low growth rates. This was confirmed by terminating the experiment prior to the growth stage, and visually inspecting the surface. Multi-colored growth rings were clearly visible; indicating the presence of a thin film measured to be approximately 300 nm thick, via FTIR. It was found that by increasing the carbonization temperature from 1140 °C to 1175 °C, and thus introducing SiH\textsubscript{4} at a higher temperature, the morphology of the films improved. In addition, SiH\textsubscript{4} was gradually introduced after carbonization as a function of temperature, to a maximum flow of 4 sccm, to help minimize defect formation during the initial growth phase. Because the majority of the deposition occurs during the growth stage, where the Si/C ratio plays a major role, this became the focus of the next set of experiments.
Table 3.1: 3C-SiC growth optimization experiments.

<table>
<thead>
<tr>
<th>Silane (sccm)</th>
<th>Propane (sccm)</th>
<th>Growth Rate (µm/h)</th>
<th>Si/C Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>6</td>
<td>10</td>
<td>0.72</td>
</tr>
<tr>
<td>16</td>
<td>7</td>
<td>14</td>
<td>0.76</td>
</tr>
<tr>
<td>18</td>
<td>8</td>
<td>16</td>
<td>0.75</td>
</tr>
<tr>
<td>23</td>
<td>10</td>
<td>18</td>
<td>0.77</td>
</tr>
<tr>
<td>28</td>
<td>10</td>
<td>22</td>
<td>0.93</td>
</tr>
<tr>
<td>35</td>
<td>11.5</td>
<td>30</td>
<td>1.01</td>
</tr>
</tbody>
</table>

Using the initial process growth conditions described in the previous section as the starting point, a series of Si/C ratio experiments were conducted (Table 3.1). First, C<sub>3</sub>H<sub>8</sub> was fixed at 6 sccm and SiH<sub>4</sub> was increased until morphology began to degrade. Once the maximum Si/C ratio was found, which resulted in specular films, both precursors were then increased, while maintaining a constant Si/C ratio, until the morphology began to degrade. Different Si/C ratios were necessary depending on the mole fractions of both SiH<sub>4</sub> and C<sub>3</sub>H<sub>8</sub>. For higher mole fractions, a larger Si/C ratio was necessary. At growth rates above 18 µm/h, the Si/C ratio had to be increased in order to maintain a specular film morphology. This is possibly due to the contribution of the particular species C<sub>3</sub>H<sub>8</sub> to the growth [51]. As described in section 2.2, simulations performed on 4H-SiC epitaxial growth by Y. Shishkin et. al, found that the particular gas species C<sub>3</sub>H<sub>8</sub>, contributed negligibly to the epi growth [24]. However, in higher concentrations it may in fact begin to affect the process, thus resulting in the need to increase the Si/C ratio to maintain process stability [51]. Figure 3.3 shows the relationship is linear between the SiH<sub>4</sub> mole fraction and growth rate. Films deposited at rates of 18 µm/h or less were of
comparable quality to each other, whereas films deposited at rates greater than 18 μm/h resulted in successive film degradation. The maximum growth rate and thickest (specular) film achieved during these experiments were 30 μm/h and 22 μm, respectively. The process schedule is identical to that described in Figure 3.2, except the carbonization temperature was 1175 °C and the growth temperature was 1385 °C.

Figure 3.3: Growth rate versus silane mole fraction.

3.2.3 Growth on 50 mm Si(100) wafers

Once the high deposition rate processes were developed, the next step was to apply them to larger surface areas, specifically 50 mm diameter Si wafers. The wafers were n-type, low resistivity, Si(100). Initial experiments found that specular growth over the entire wafer was not possible due to a large temperature gradient in the hot zone. Lower temperatures at the inlet caused deposition on the upstream portion of the wafer to be polycrystalline, whereas higher temperatures at the outlet caused the downstream portion of the Si wafer to melt. Through a series of melt tests, whereby a drop of Si is melted to calibrate the hot zone temperature reading of the pyrometer, it was determined that the temperature gradient was approximately 35 °C along the length of the 50 mm
growth zone (see Figure 3.4). It was suggested that, by increasing the length of the hot zone and the volume of the insulating graphite foam, the temperature gradient could be reduced [51]. By having a longer hot zone, as shown in Figure 3.4 (b), the gases would have more time to heat up and reach a steady-state temperature and the increase in volume of the insulating foam would help to maintain hot zone heating uniformity. The length of the hot zone was increased by ~32% and the overall volume of the insulating foam was increased by nearly 100%. This resulted in a less than 5 °C difference across the length of the 50 mm growth zone. Further details of the hot zone design can be found in Appendix A. The growth was conducted in the same manner described in the previous section. The growth process on the 50 mm Si wafers was found to be more affected by the condition of the CVD reactor and hot zone, than growth on the die. Because of the larger surface area of the wafers and the temperature gradient inside the hot zone, the temperature window for single crystal growth was smaller. Completely specular films could only be obtained in the range between 1380 °C and 1390 °C; below 1380 °C polycrystalline areas formed on the edges of the wafers, and above 1390 °C the wafer edges began to melt. If the same graphite foam was used for too long of a period and it began to degrade, the temperature gradient worsened. Also, if the CVD reactor had remained idle for several days, a conditioning run was usually necessary. The conditioning run entailed performing the baseline process (deposition rate of 10 μm/h) for 10 to 15 minutes on a Si die.
3.2.4 Intentional doping of the 3C-SiC films

Once the 3C-SiC growth on 50 mm diameter Si wafers was successful, intentional doping experiments of the 3C-SiC films were then conducted. Nitrogen (N$_2$) mixed in H$_2$ was used as an n-type dopant. In the first experiment, 100 sccm of a 1% N$_2$ in H$_2$ mix was used to obtain a doping value around $10^{16}$ cm$^{-3}$. In the second experiment, 50 sccm and 100 sccm of a 10% N$_2$ in H$_2$ mix was used to obtain a doping value around $10^{17}$ cm$^{-3}$. Figure 3.5 shows the correlation between the N$_2$ mole fraction and the doping of the 3C-SiC films. The ability to achieve variously doped 3C-SiC epilayers is an important step in developing 3C-SiC based electronic devices. Intentionally doped 3C-SiC films produced from this work will be used to fabricate a 3C-SiC MOSCAP (see section 4.3).
Figure 3.5: $N_2$ mole fraction versus carrier concentration of the 3C-SiC films.

3.3 3C-SiC Film Characterization

The thickness of the 3C-SiC epilayers was assessed with Fourier Transform infrared (FTIR) spectroscopy, and confirmed by cross-section scanning electron microscopy (SEM). The SEM cross-sections were also used to investigate the 3C-SiC/Si interface. Surface morphology was inspected via Nomarsky interference optical microscopy, atomic force microscopy (AFM), and SEM. The quality of the crystalline films was determined through X-ray diffraction (XRD) and low-temperature photoluminescence (LTPL) analysis. A non-contact mercury probe was employed to perform the CV/IV measurements, and the doping profiles of the grown 3C-SiC films.

3.3.1 FTIR

The thickness of the epitaxially grown layers was measured with an Accent [52] QS1200 model FTIR. The FTIR uses a directed IR beam which passes through the epilayer and reflects off of the substrate creating, a primary and secondary interferogram. This signal is then subtracted from a reference sample and the thickness of the film is
determined. A major benefit in using an FTIR is the ability to make quick, non-destructive and accurate thickness measurements, which allows the measurement of many points on the film to determine growth uniformity. Measurements of the 8 x 10 mm die were taken at the center of the die to try and avoid variations due to edge effects. Measurements of the 50 mm wafers were collected at five points, as illustrated in Figure 3.6. Variations in thickness across all measured wafers were found to be less than 15%. Table 3.2 contains thickness measurements taken of two 3C-SiC epi-layers deposited at 18 μm/h and 30 μm/h. Note the decrease in film thickness along the direction of the gas flow (A to E); this is likely attributed to the partial depletion of species along the gas stream. Also, the film deposited at the higher rate had less variation in thickness across the wafer, 5.5% compared to 12.7%. This is probably due to the higher mole fractions of SiH₄ and C₃H₈ present in the higher deposition rate process. The deposition rate was calculated by measuring the thickness for a particular growth time, subtracting 0.4 μm for the epilayer grown during the second temperature ramp, and multiplying by a factor to determine the rate in μm/h. A slight decrease in deposition rate and an improvement in morphology were observed when transferring the growth process from 8 x 10 mm die to 50 mm wafers. For example, a particular process which yielded 20 μm/h on the die, yielded 18 μm/h when applied to a 50 mm wafer. These results remained consistent throughout numerous experiments. Details on how the size of the growth area affected morphology can be found in the next section.
Table 3.2: Thickness measurements taken on two wafers deposited at different growth rates. Thickness measured via FTIR reflection spectroscopy.

<table>
<thead>
<tr>
<th>Point</th>
<th>Thickness (μm) rate = 18 μm/h</th>
<th>Thickness (μm) rate = 30 μm/h</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>10.4</td>
<td>11.3</td>
</tr>
<tr>
<td>B</td>
<td>9.5</td>
<td>10.8</td>
</tr>
<tr>
<td>C</td>
<td>9.7</td>
<td>10.8</td>
</tr>
<tr>
<td>D</td>
<td>9.4</td>
<td>10.7</td>
</tr>
<tr>
<td>E</td>
<td>9.2</td>
<td>10.8</td>
</tr>
</tbody>
</table>

Figure 3.6: Diagram of wafer mapping for thickness measurements shown in Table 3.2.

3.3.2 Optical microscopy

A Normarski interference optical microscope was used to visually inspect the surface of the 3C-SiC epilayers. The available objectives ranged from 100 to 500 times magnification. Figure 3.7 (a) and (b) are optical images of 3C-SiC films taken at 500X using the same growth process and deposition rate, applied to an 8x10 mm die and a 50 mm wafer, respectively. From these images one can clearly see how the surface of the film improves when depositing on larger growth areas. Figure 3.7 (c) and (d) are optical images of 10 μm thick 3C-SiC films at 500X, which were deposited at different growth rates on 50 mm wafers. A higher concentration of hillocks can be seen on the film deposited at 30 μm/h (Figure 3.7 (d)) compared to the one deposited at 18 μm/h (Figure 3.7 (c)). Note also the larger size of the hillocks in the film deposited at the higher growth rate. The hillock defect densities were approximately 1.9 x 10^4 cm^-2 and 0.23 x 10^4 cm^-2, respectively. These values are comparable to, and in the case of the film deposited at 18 μm/h, better than those reported in the literature [20].
Figure 3.7: Optical images taken at 500X of (a) 5.4 µm thick film deposited at 18 µm/h on 8x10 mm die (b) 5 µm thick film deposited at 18 µm/h on 50 mm wafer (c) 10 µm thick film deposited at 18 µm/h on 50 mm wafer (d) 10 µm thick film deposited at 30 µm/h on 50 mm wafer.

3.3.3 SEM

A Hitachi [53] model SEM at the USF COT facility in Largo, FL [54] was used to confirm the FTIR thickness measurements and investigate the 3C-SiC/Si interface. Cross-sections taken of several films with varying thickness and deposition rates found very few voids present at the 3C-SiC/Si interface. Figure 3.8 is a cross-section of a 10 µm thick film deposited at 30 µm/h, and no voids are visible at the 3C-SiC/Si interface. The near absence of voids is likely attributed to the longer ramp-up and cool-down times used during the growth of the crystalline films.
Cross-section SEM was also employed in the investigation of the hillock defects. A 3C-SiC film with a high density of hillocks was chosen for study. The sample was prepared by mechanically polishing the edge with diamond impregnated paper. With each polish, a finer grit size was used, until the edge was mirror-like. This edge was then studied under the SEM, using both secondary and backscattered electrons. Figure 3.9 (a) and (b) are SEM backscatter electron images of a hillock cross-section. Root-like features can be seen penetrating down into the crystal from the hillock. From the SEM images, it is not clear what initiates the defect formation; possibly dislocations in the crystal growth or precipitates interrupting the nucleation. Whatever the cause, it is apparent that hillocks extend beyond the surface into the epitaxial layer.
3.3.4 AFM

A Veeco Digital Instruments [55] model AFM was used to quantify the surface morphology of the grown films. An AFM is a type of scanning probe microscope which employs a cantilever and laser feedback system. As the cantilever passes over the sample surface, a position sensitive photo detector measures the changes in the laser signal and creates a topographical representation of the surface. For all of the surface studies, tapping mode AFM was used. Figure 3.10 (a) and (b) are 50 x 50 μm scans, taken at a z-height of 100 nm, of films grown at 18 μm/h and 30 μm/h, respectively. Note the slightly larger grain sizes in Figure 3.10 (a). AFM and optical data would suggest the film deposited at 18 μm/h was of higher quality than the film deposited at 30 μm/h. However, despite the lower hillock defect density and smoother surface, XRD and LTPL analysis suggests the crystalline structure to be slightly superior in the film deposited at 30 μm/h.
Figure 3.10: 50 x 50 μm AFM scans of 10 μm thick 3C-SiC films on 50 mm Si wafers, deposited at: (a) 18 μm/h and (b) 30 μm/h. Tapping mode with a z-height of 100 nm was used. Images courtesy of D. Edwards, USF-COT, Largo, FL.

3.3.5 XRD

XRD was used to analyze the crystalline quality of the 3C-SiC films deposited on the 50 mm Si(100) wafers. In XRD, x-rays are used to determine the normal spacing between adjacent crystallographic planes by means of Bragg’s law. If a crystal has few defects, then less scattering of the x-rays will occur, and the intensity peak of the reflected beam will be narrow [56]. The epitaxial layers were not removed from the substrate prior to measurement. Powder diffraction measurements, in which the sample is scanned over a wide range of angles, were taken first, in order to determine the orientation of the grown layers. Figure 3.11 (a) and (b) are powder diffractions taken on 10 μm thick 3C-SiC on Si(100) films deposited at 18 μm/h and 30 μm/h, respectively. Note the strongest peaks for both films occur at approximately 41°, which corresponds to the <200> plane of 3C-SiC. Additional peaks can be found at approximately 90° and 69°. These peaks corresponds to the <400> plane of 3C-SiC and the <200> plane of cubic Si, respectively. The presence of a peak at 69° is likely due to the X-Rays penetrating through the 3C-SiC film and diffracting off of the underlying Si substrate. No other peaks were present, confirming that the grown epitaxial layers are single crystal
3C-SiC oriented in the <100> direction. Figure 3.11 (c) and (d) are rocking curve measurements taken on the <200> 3C-SiC peak. The full-width half-maximum (FWHM) values were slightly improved in the higher growth rate process; the FWHM was measured to be 300 arcseconds, compared to a FWHM of 340 arcseconds. Theses values were found to be comparable [25] and in several cases better [27,57] than those reported in literature.

![Figure 3.11: XRD of 10 μm thick 3C-SiC epilayers on 50 mm Si(100) wafers. Powder diffraction of films deposited at: (a) 18 μm/h and (b) 30 μm/h. Rocking curve of the 3C-SiC(200) peak of films deposited at: (c) 18 μm/h and (b) 30 μm/h.](image)

3.3.6 LTPL

Two samples of the epitaxially grown 3C-SiC films, deposited at 18 μm/h and 30 μm/h, were sent to Dr. Choyke’s group at the University of Pittsburgh for LTPL (2 K)
analysis. The results indicate that the film deposited at the higher growth rate is of slightly better quality than the lower growth rate film. Details of the measurements can be found in Appendix B.

3.3.7 CV/IV

A mercury (Hg) probe was used to make non-contact CV and IV measurements of the as grown 3C-SiC films. Figure 3.12 is a plot of the current versus voltage for a 10 µm thick, unintentionally doped 3C-SiC film. The voltage was swept from -3V to 3V using front to back contacts. The results clearly indicate the 3C-SiC film is n-type.

Figure 3.12: Plot of the log of the current vs. voltage of an unintentionally doped 10 µm thick 3C-SiC film. The film is clearly n-type. Note measurements made A to C (inset shows device cross-section). Anode contact, A, made via Hg probe.

Once the IV characteristics were determined, the capacitance versus voltage was measured for the same film by making front to front contacts and applying a reverse bias (see Figure 3.13). The reverse bias creates a depletion region of width W, which is dependent on the applied voltage [58]. From this relationship, the carrier concentration of the film can be determined. Figure 3.14 is the plot of the calculated carrier
concentration versus depth (W) of the 3C-SiC film. The carrier concentration was estimated to be around $10^{15}$ cm$^{-3}$; this value remained consistent for all the unintentionally doped 3C-SiC films that were measured.

![Figure 3.13](image)

Figure 3.13: Plot of capacitance vs. voltage for an unintentional doped n-type, 10 μm thick 3C-SiC film. Inset shows device cross-section. Note measurement made A to C.

![Figure 3.14](image)

Figure 3.14: Plot of calculated carrier concentration vs. depth for an unintentional doped n-type, 10 μm thick 3C-SiC film. A doping density of N$_D$-N$_A$ ~ $10^{15}$ cm$^{-3}$ was estimated for this film.

The CV and IV plots shown above were from measurements taken at the center of the 50 mm diameter wafer. A doping density of N$_D$-N$_A$ ~ $10^{15}$ cm$^{-3}$ was estimated for this film. Additional measurements were taken on various points across the wafer (see Figure 3.15)
to determine the doping uniformity. There were slight variations in doping across the 50 mm wafers, with higher values on the upstream portion of the wafers.

Table 3.3 shows the variations in doping for two 3C-SiC films grown at different deposition rates. This could possibly be due to preferential depletion of certain species along the gas stream, resulting in slight variations across the wafer in the Si/C ratio. It is clear from the values listed in the table below, that the lower deposition rate process resulted in a more uniform doping profile than the higher deposition rate process.

<table>
<thead>
<tr>
<th>Point</th>
<th>$N_D-N_A \times 10^{15}$ cm$^{-3}$ rate = 18 $\mu$m/h</th>
<th>$N_D-N_A \times 10^{15}$ cm$^{-3}$ rate = 30 $\mu$m/h</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.4</td>
<td>4.6</td>
</tr>
<tr>
<td>B</td>
<td>3.2</td>
<td>3.2</td>
</tr>
<tr>
<td>C</td>
<td>3.1</td>
<td>4.5</td>
</tr>
<tr>
<td>D</td>
<td>3.2</td>
<td>3.2</td>
</tr>
<tr>
<td>E</td>
<td>3.2</td>
<td>5.1</td>
</tr>
</tbody>
</table>

**Figure 3.15:** Diagram of wafer mapping for doping measurements shown in Table 3.3.

### 3.4 Summary

A stable 3C-SiC heteroepitaxial growth process on Si substrates, with deposition rates up to 30 $\mu$m/h, has been developed. First, a baseline process was achieved; the 3C-SiC films were specular, but the deposition rate was low (~ 10 $\mu$m/h). The baseline process was then optimized through temperature, pressure, and Si/C ratio experiments. With the optimized process, thick 3C-SiC films (up to 22 $\mu$m thick) and high deposition rates (up to 30 $\mu$m/h) were obtained. Next, the optimized process was applied to growth on 50 mm diameter Si(100) wafers. Before large area growth could be achieved, the CVD
reactor was modified to reduce the temperature gradient from \(~35\) °C to \(~5\) °C in the growth zone. This resulted in the ability to produce specular films on 50 mm diameter Si(100) wafers. Growing over the larger areas has helped to reduce defects and improve production, which is an important step for 3C-SiC device research.
4.1 Growth on Wafer-Bonded Films (SOI)

Now that a repeatable high deposition rate 3C-SiC on Si process has been established on 50 mm diameter wafers, efforts are underway to apply the grown films in numerous applications, such as growth on wafer-bonded films (SOI). One of the disadvantages of 3C-SiC heteroepitaxy is that growth temperature is limited by the melting point of the underlying Si substrate, which is approximately 1410 °C. In recent years, interest has surfaced in developing 3C-SiC processes on novel substrates. Work was done in this field by R.L. Myers-Ward at USF, and one of the substrates she investigated was wafer-bonded silicon on insulator (SOI) [31]. SOI typically consists of a thin layer of Si bonded to a semi-insulating or insulating substrate, such as polycrystalline SiC [59,60]. The advantage of using SOI substrates is that the thin layer of Si is consumed during growth, thereby allowing high temperature growth to proceed. SOI technology is also advantageous to device fabrication; the insulating layer helps to reduce power consumption and increase speeds in IC’s [60]. The following work picks up where Dr. Myer’s research left off.
The SOI substrates consisted of a thin layer of (001)Si, directly bonded onto a polycrystalline SiC substrate using the SmartCut® technique (Figure 4.1). The SOI substrates were provided by M. Sherwin at Northrop Grumman [62] in several batches with the Si layer varying from 0.3 μm to 1 μm thick. Samples were cut into 8x10 mm die and prepared in the same manner described in section 3.2.1. In all of the CVD experiments, a bare Si(100) control sample was placed along side the SOI samples. Batch 1 consisted of the 1 μm thick Si layer, and was the initial sample used. The experiment was conducted using the low deposition rate (10 μm/h) process described in section 3.2.1. It was found that the Si layer was too thick, and all attempts resulted in polycrystalline 3C-SiC growth even though the control samples were always single crystal. Batch 2 consisted of SOI with 0.5 μm thick Si layers. Specular growth, up to 2 μm thick, was achieved on these samples. The following three batches: Batch 4 (0.3-0.4 μm thick), Batch 5 (0.4-0.5 μm thick), and Batch 6 (0.5-0.6 μm thick), contained some thinner Si layers for the purpose of high temperature growth. Growth on all three of these batches resulted in crystalline films. Figure 4.2 (a) is an SEM surface image of a 1 μm thick 3C-SiC film, deposited at 10 μm/h, on a 0.5 μm thick SOI substrate. Although the surface was specular, it was found to be highly grainy under SEM. Figure 4.3 (b) is
an SEM surface image of an 11 μm thick 3C-SiC film, deposited at 14 μm/h, on a 0.4 μm thick SOI substrate. It is clear from the images that the thicker film is of higher quality.

Figure 4.2: SEM images taken at 5,000X of: (a) 1 μm thick 3C-SiC epi on SOI substrate, and (b) 11 μm thick 3C-SiC epi on SOI substrate.

The challenge to performing high temperature growth was determining when the entire Si layer had been consumed. Several experiments were conducted to produce films of varying thickness, which were then examined via cross-section SEM to determine if any of the Si remained. It is critical that the entire Si layer is consumed before high temperature growth is attempted, otherwise melting of the Si can cause bubbles to appear on the surface of the film. Figure 4.3 (a) is a SEM cross-section of a 1 μm thick 3C-SiC epilayer, and clearly shows the presence of a Si layer between the epi and polycrystalline substrate. Figure 4.3 (b) is a SEM cross-section of an 11 μm thick 3C-SiC epilayer with no Si remaining between the epi and the polycrystalline substrate.
Figure 4.3: SEM cross-section of: (a) 1 μm thick 3C-SiC epi on SOI substrate, with Si layer present, and (b) 11 μm thick 3C-SiC epi on SOI substrate with no Si layer present.

Figure 4.4: Process schedule developed for high temperature growth of 3C-SiC on SOI.

Once the initial Si layer is consumed in the first stage of growth, the temperature is increased and a second stage of growth is conducted (Figure 4.4). The first stage of growth was conducted at 1385 °C for 45 minutes, followed by 15 minutes at the higher temperature. Temperatures of 1450 °C, 1500 °C and 1550 °C were used for the second stage, and the effects on morphology and growth rate were compared. Figure 4.5 shows a
slight increase in the growth rate of about 0.5 μm/h for every 50 °C. The morphology however, was similar under an optical microscope for all three temperatures.

Figure 4.5: Growth rate of 3C-SiC on SOI as a function of temperature.

Although growth rates as high as 30 μm/h have been achieved on bare Si(100) substrates, it was found that 18 μm/h was the maximum growth rate possible to maintain single crystal growth on the SOI substrates. In section 3.3.2 it was shown that growth performed on 50 mm diameter Si(100) wafers had a significant improvement in morphology over growth on 8x10 mm die. Therefore, it is likely that if the 3C-SiC on SOI process was applied to a 50 mm diameter SOI wafer the quality of the 3C-SiC film would improve.

4.2 MOSCAPs

Several of the 3C-SiC films described in this thesis work, which were grown on 50 mm diameter Si(100) wafers, are currently being used in the fabrication of MOSCAPs. The following 3C-SiC films were chosen as substrates for the MOSCAPs: a 10 μm thick
unintentionally doped film, with a carrier concentration of \(10^{15} \text{ cm}^{-3}\); and a 12 \(\mu\text{m}\) thick intentionally doped film, with a carrier concentration of \(10^{16} \text{ cm}^{-3}\). Both films were deposited at a rate of 18 \(\mu\text{m/h}\). The 3C-SiC epilayers were sent to NovaSiC [63] for chemical mechanical polishing, or CMP. The oxidation, fabrication and testing of the device will be performed here at the University of South Florida (USF), by A. Joseph, I. Haselbarth, and E. Short. Simulations of the MOSCAP in Medici are being conducted by A. Joseph [64].

4.3 MEMS

3C-SiC heteroepitaxial layers have been successfully grown on MEMS molds, using \(\text{C}_3\text{H}_8/\text{SiH}_4/\text{HCl}\) precursor chemistry [65]. The experiments were conducted by M. Reyes, M. Waites, S. Harvey, Y. Shishkin, and S.E. Saddow here at USF, using the same CVD reactor described in this work. The substrates, provided by M. Waits at the Army Research Laboratory (ARL) [66], were 22, 52, and 123 \(\mu\text{m}\) deep, DRIE etched Si(100), MEMS structures. The two stage, carbonization plus growth step process was used to deposit the 3C-SiC films. Carbonization was conducted at 1115 \(^\circ\text{C}\) for 2 minutes at atmospheric pressure, and growth was conducted at 1375 \(^\circ\text{C}\) at a pressure of 100 Torr. The Si/C and Si/Cl ratios used during growth were 0.9 and 1.5, respectively. Figure 4.6 (a) and (b) are SEM images of the cross-section of a 52 \(\mu\text{m}\) deep trench before and after the 3C-SiC deposition, respectively. In Figure 4.6 (b), the thickness of the 3C-SiC layer is greater along the top and edge of the mold compared to the base. If the thickness of the film were to increase, a key-holing effect would eventually occur. New Si MEMS structures are being designed to eliminate this problem by angling the trench side-walls, at which point deposition experiments will continue.
Figure 4.6: SEM cross section of 52 \( \mu \)m deep trench in Si mold: (a) before deposition and, (b) after deposition of 3C-SiC \[65\].

4.4 3C-SiC/SOI Gas Sensor

A resistive hydrogen gas sensor was fabricated on a 3C-SiC film deposited during the course of this research, on a SOI substrate \[67\]. A 1.4 \( \mu \)m thick 3C-SiC film was deposited on a 15 nm thick Si layer bonded to polycrystalline SiC, using a growth process similar to that described in 3.2.1. The fabrication and testing of the device was performed by Dr. T. J. Fawcett at both the USF and COT facilities in Tampa and Largo, FL. A 5000 Å thick SiO\(_2\) layer was deposited via PECVD, followed by etching of the active area, and metal contact deposition. After deposition, the contacts were annealed to produce ohmic-like behavior. The samples were then sent to A.L. Spetz at Linköping University, Sweden to be packaged. When tested, the device was capable of detecting 10% to 100% H\(_2\) concentration in N\(_2\), at a temperature of 673 K.
Baseline and optimized 3C-SiC epitaxial growth processes on (100)Si were developed during this thesis work. These processes have been applied to growth on bonded substrates (SOI), and the fabrication of MOSCAPs, MEMS, and gas sensors. The SOI substrates with thin layers of Si, ranging from 0.3 μm to 1 μm thick, were bonded to polycrystalline SiC. Crystalline growth was achieved on all but the 1 μm thick sample. Additional high temperature (>1410 °C) experiments were also conducted, which resulted in an increase in the growth rate of about 0.5 μm/h per 50 °C. The samples provided for the MOSCAPs were two 50 mm diameter 3C-SiC on Si(100) wafers, with doping values of \(~10^{15}\) cm\(^{-3}\) and \(~10^{16}\) cm\(^{-3}\). 3C-SiC epitaxial growth was also achieved on 22, 52, and 123 μm deep, DRIE etched Si(100), MEMS structures, provided by ARL [65]. The growth process used on the molds was similar to the baseline process, with the addition of HCl to the precursor chemistry. Because key-holing effects prevented the filling of the trenches, new molds are being fabricated with angled side-walls.
CHAPTER 5  CONCLUSIONS AND FUTURE WORK

5.1 Summary

A 3C-SiC heteroepitaxial CVD growth process on 50 mm diameter Si(100) substrates, with deposition rates up to 30 μm/h, has been developed and characterized during this thesis work. The growth process was developed in three stages; an initial “baseline” development stage, an optimization stage, and a large area growth stage.

The baseline process was achieved using a two step growth method. First the sample was heated from room temperature to 1140 °C, at atmospheric pressure, using a H\textsubscript{2}/C\textsubscript{3}H\textsubscript{8} (10 slm/6 sccm) gas mixture. The temperature was maintained at 1140 °C for 2 minutes to carbonize the Si surface. Then SiH\textsubscript{4} was introduced into the gas mixture at a flow rate of 4 sccm, and the temperature increased to 1375 °C, which is the growth temperature. Once the growth temperature was reached, the pressure was lowered to 100 Torr and H\textsubscript{2} and SiH\textsubscript{4} were increased to 30 slm and 13 sccm, respectively. The resulting 3C-SiC films were specular, but the deposition rate was low (~ 10 μm/h).

The baseline process was then optimized through temperature and Si/C ratio experiments. The growth was conducted in the same manner as the baseline process. However, the carbonization temperature was raised to 1175 °C and SiH\textsubscript{4} was introduced incrementally during the second temperature ramp. During growth, the C\textsubscript{3}H\textsubscript{8} and SiH\textsubscript{4} mole fractions were significantly increased. With the optimized process, thick 3C-SiC films (up to 22 μm thick) and high deposition rates (up to 30 μm/h) were obtained.
Finally, the optimized process was applied to growth on 50 mm diameter Si(100) wafers. Before large area growth could be achieved, the CVD reactor was modified to reduce the temperature gradient from \( \sim 35 \, ^\circ C \) to \( \sim 5 \, ^\circ C \) in the effective growth zone (see Figure 3.4). This resulted in the ability to produce specular films on 50 mm diameter Si(100) wafers. There was a slight decrease in the growth rate, but a significant improvement in the surface morphology when the process was transferred from the 8 x 10 mm die to the 50 mm diameter wafers.

The 3C-SiC films grown during this work were characterized using a variety of methods. The thickness of the 3C-SiC epilayers was assessed through Fourier Transform infrared (FTIR) spectroscopy, and confirmed by cross-section scanning electron microscopy (SEM). The SEM cross-sections were also used to investigate the 3C-SiC/Si interface and study hillock defects. There were very few voids found at the epi/substrate interface. Cross-sections of the hillocks revealed root-like features penetrating down into the epitaxial layer. However, the cause and origin of these defects could not be determined without further investigation. The surface morphology of the films was inspected via Nomarsky interference optical microscopy, atomic force microscopy (AFM), and SEM. The density of the hillock defects was estimated to be between \( 1.9 \times 10^4 \) cm\(^{-2} \) and \( 0.23 \times 10^4 \) cm\(^{-2} \), depending on the deposition rate. The surface defects became larger and denser with higher deposition rates and thicker films. The crystalline quality of the 3C-SiC films was determined through X-ray diffraction (XRD), performed at USF, and low-temperature photoluminescence (LTPL) analysis, performed at the University of Pittsburgh. Results from the powder diffraction measurements revealed peaks only from the \(<200>\) and \(<400>\) 3C-SiC and \(<200>\) Si crystallographic planes,
indicating that the epitaxially grown layers are cubic SiC. Rocking curve measurements on the <200> 3C-SiC peak of two 10 μm thick films, deposited at different rates, resulted in FWHM values of 300 and 340 arcsec. The narrower peak corresponded to the film grown at the higher deposition rate, indicating possibly a higher quality crystalline structure. This was confirmed by the LTPL (2 K) measurements. A mercury probe was used to make non-contact CV/IV measurements of the 3C-SiC films. It was determined from the IV measurements that the films were n-type. Doping densities of $10^{15}$ and $10^{16}$ were extracted from the CV measurements for the unintentionally and intentionally doped films, respectively. There were slight variations in doping across the films deposited on 50 mm diameter Si wafers. Overall, the 3C-SiC films grown during this work were of comparable quality to the best films reported in the literature.

The 3C-SiC CVD processes developed during this work, and many of the grown 3C-SiC films, were used in numerous applications. The baseline process was used to deposit 3C-SiC films on MEMS structures with 22, 52 and 123 μm deep trenches. The optimized process was used to conduct high temperature 3C-SiC epitaxy on Si bonded to polycrystalline SiC (SOI) substrates. Also, a 3C-SiC on SOI film was used in the fabrication of a wide-range resistive H$_2$ gas sensor and two 3C-SiC films deposited on 50 mm Si wafers were used in the fabrication of MOSCAPs.

5.2 Future Work

The development of a high growth rate 3C-SiC epitaxial process, and the ability to deposit films over 50 mm diameter Si wafers, which has helped to reduce defects and improve production, is an important step in the on-going SiC research being conducted here at USF. However, the optimization process is never “complete”; there are many
techniques available to try and further improve the 3C-SiC growth process. Currently, M. Reyes is investigating the addition of HCl to the SiH\textsubscript{4}/C\textsubscript{3}H\textsubscript{8} precursor mix, and shortly experiments will begin to develop a 3C-SiC growth process using methylchloride (CH\textsubscript{3}Cl) in addition to the standard chemistry. A second CVD reactor has been built, by C. Frewin in our group and work will soon begin to establish a 3C-SiC growth process on 100 mm diameter Si wafers. Also in collaboration with O. Kordina at Caracal [68], work has begun to grow a thick (+100 μm) 3C-SiC layer, using the 18 μm/h deposition process developed during this thesis, for use as a seed wafer for the growth of bulk 3C-SiC crystals.

One of the challenges affecting the bulk growth process is the inability to grow high quality thick films (> 50 μm) of 3C-SiC on Si. The thicker the 3C-SiC films become, the greater the density of surface defects, to the point in which the surface is no longer specular. The likely culprits are the lattice mismatch between 3C-SiC and Si and precipitates in the reactor. The precipitates could be minimized by following a more rigorous reactor cleansing schedule, such as cleaning the reactor after every growth run, and/or swapping out graphite parts sooner, so that degradation is not an issue. However, the cost of parts can make this an uneconomical solution. There also is the matter of the lattice mismatch at the 3C-SiC/Si interface, which causes stress in the epitaxial layer and can lead to the formation of defects. Unlike SiGe, 3C-SiC can not alloy with Si to form a defect-free buffer layer between the two materials. Figure 5.1 (a) illustrates how Si and Ge can be alloyed to create a buffer layer between the two materials. Note the difference at the interface in the case of 3C-SiC layer on Si (Figure 5.1 (b)). One way in which defects due to the stress at the interface could possibly be reduced is by growing a
compliance layer between 3C-SiC and Si (Figure 5.1 (c)). If a thin 3C-SiC layer could be degenerately doped with larger substitutional atoms, so that the lattice constant is larger than that of an unintentionally doped 3C-SiC film, it could serve as an intermediate layer between the Si substrate and 3C-SiC epi. Another way defects could possibly be reduced is by growing in stages. First, an initial 3C-SiC layer would be grown using a low deposition rate process to produce a high quality thin film (1-2 μm thick). This would be followed by a short H₂ etch to clean the surface and a cool down to room temperature. Finally, the sample would be re-grown on without breaking vacuum, using a higher deposition rate process. The H₂ etch and cool down could be repeated periodically, say every 45-60 minutes, to try and minimize the propagation of defects. Whether or not these suggestions can improve the current growth process has yet to be determined. The key to ensuring that 3C-SiC research here at USF remains on the forefront, is to continue finding ways to improve the growth process.

Figure 5.1: Illustration of: (a) SiGe epitaxy on Si, with a graded SiₓGe₁₋ₓ alloy layer in between (b) 3C-SiC epitaxy on Si, and (c) 3C-SiC epitaxy on Si, with a degenerately doped 3C-SiC layer in between to serve as a buffer layer.
REFERENCES


[51] Personal communication with Y. Shishkin, 10 July 2006.


APPENDICIES
Appendix A  Hot Zone Design Drawings

Figure A.1: Original design of insulating graphite foam used in the development of the baseline and optimized 3C-SiC processes on Si die. The graphite susceptor is shown in A.3. All units are shown in mm. Drawing courtesy of I. Haselbarth, USF, Tampa, FL.
Figure A.2: Modified design of insulating graphite foam used during the development of the 3C-SiC growth process on 50 mm diameter Si wafers. The graphite susceptor is shown in A.4. All units are shown in mm. Drawing courtesy of I. Haselbarth, USF, Tampa, FL.
Appendix A (Continued)

Figure A.3: Original design of tilted susceptor (only top shown here) used in the development of the baseline and optimized 3C-SiC process on Si die. All units shown in mm. Drawing courtesy of I. Haselbarth, USF, Tampa, FL.

Figure A.4: Modified design of tilted susceptor (only top shown here) used in the development of the 3C-SiC growth process on 50 mm diameter Si wafers. All units shown in mm. Drawing courtesy of I. Haselbarth, USF, Tampa, FL.
Appendix B  Low Temperature Photoluminescence (LTPL)

Two 3C-SiC samples were sent to W.J. Choyke at the University of Pittsburgh for low temperature photoluminescence (LTPL) analysis [69]. Both samples were 3C-SiC layers, approximately 10 \( \mu \text{m} \) thick, on Si(100) substrates, which were cut into 1 cm x 1 cm die from a 50 mm diameter wafer. The two films were grown at different deposition rates; one at 18 \( \mu \text{m/h} \) and the other at 30 \( \mu \text{m/h} \). The measurements were conducted at a temperature of 2 K. The excitation source was a 40 mW He-Cd ion laser, operating at a wavelength of 325 nm, and the detector was a UV sensitive CCD-9000. Details of the experimental setup can be found in [69]. At a wavelength of 325 nm, the light penetration depth into 3C-SiC is 2.9 \( \mu \text{m} \). Therefore, the laser source was suitable for the 10 \( \mu \text{m} \) thick 3C-SiC films because the influence of the underlying Si substrate on the detected LTPL spectrum was minimal. Figure B.1 (a) and (b) below are the measured PL spectrums from the 3C-SiC films deposited at 18 \( \mu \text{m/h} \) and 30 \( \mu \text{m/h} \), respectively. The spectrum of the film deposited at 30 \( \mu \text{m/h} \) (Figure B.1 (b)) has a better signal to noise ratio and stronger L_\text{A} peak, than the film deposited at 18 \( \mu \text{m/h} \) (Figure B.1 (a)). However, both near-band-edge spectra did not exhibit the N_0 zero-phonon line. The peaks labeled (2) are attributed to the D_{\text{H}} intrinsic defect which normally occurs at 5373 Å, but due to stress in the epilayer there is likely a red-shift.
Figure B.1: LTPL (2 K) spectrum of 10 μm thick 3C-SiC film deposited at: (a) 18 μm/h and (b) 30 μm/h. Images courtesy of W.J. Choyke, University of Pittsburgh, PA.